Spatial Analysis of Ring Oscillator Devices

A. Somani, L. W. Teo, and D. S. Boning, *Member, IEEE*

***Abstract*— Spatial dependencies tend to introduce correlations among parameter values obtained from test structures. These spatial correlations obscure the parameter correlations caused by common underlying variables and make process diagnosis more difficult. In this work, linear regression method has been used to generate the spatial models for both wafer and chip level to investigate their significance. It is found that the wafer level regression model does not have a strong wafer level dependence on the ring oscillator devices. On the other hand, at the chip level, goodness of fit calculated for certain device structures exhibit strong spatial dependence on the linear regression model. This proves that it is essential to consider different levels of spatial dependence before making conclusion on the variations caused by underlying variables and parameter.**

***Index Terms*—Spatial analysis, linear regression, least square method**

I. Introduction

SINCE the birth of the integrated circuit nearly four decades ago, the semiconductor industry has distinguished itself from the other industries by its rapid pace of improvement. Most of the improvements on its products have resulted essentially from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. As device dimensions reduce and wafer sizes increase, process uniformity is becoming an increasingly important and difficult task. A sound understanding of variations, particularly spatial variation, is essential to both control the process and to design manufacturable circuits [1]-[4]. Some process variations, such as line-width changes of poly or interconnect, can significantly affect circuit performance. This requires the development of new techniques to measure and extract variation in a given process and link it to circuit performance.

Test circuits are normally designed to add intentional variations in device parameters. These variations are carefully controlled in terms of their magnitude as well as their behavior towards expected process variations. However, different degree of spatial dependence on either the wafer level or chip level may distort the results drawn from these devices measurements. Therefore, in order to infer any reliable models or draw any conclusions, any possible trends of spatial correlation with the measured results have to be deconvoluted. Examples of common spatial dependencies for unrelated process parameters could be radical dependence of crystal point defects, ion implantation incidence angle, and photoresist thickness.

Since variation is manifested in several forms, the main aim of this paper is to identify any wafer level or chip level spatial dependence that would affect the conclusions drawn from any device measurements.

II. Problem Formulation

The present work focuses on establishing a relation between spatial variance with observed parameters such as frequency of ring oscillators in chip. Ring Oscillators (ROs) are standard test structures to determine the delay in different process. The chip architecture used in this paper is based on the design by Panganiban [5] and the testing methodology used to generate the raw data is clearly explained by Gonzalez [6]. The chips were manufactured by TSMC using 0.25 μm MOSIS [7]. Fig. 1 shows the chip locations within the wafer that the data are analyzed. Note that all the chips are obtained from the top half of the wafer and a majority of them were from the top left hand side of the wafer.

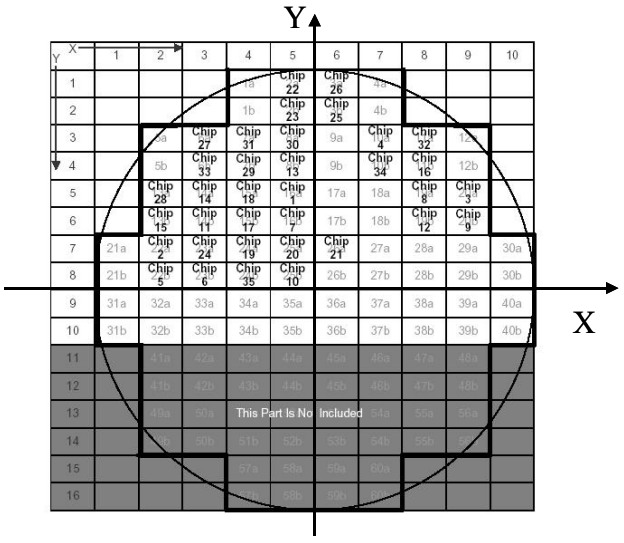

Fig. 1. Spatial location of wafer [6]

Manuscript received May 14, 2003. This work was supported by NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing and Singapore-MIT Alliance research grant.

A. Somani is with the Microsystems Technology Laboratories, Department of Material Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139, USA.

L. W. Teo is with the Advance Materials Micro- and Nano- Systems programme, Singapore-MIT Alliance, 4 Engineering Drive 3, Singapore 117576.

D. S. Boning is with the Microsystems Technology Laboratories, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139, USA.

Typical test structures found in each chips are normally divided into two types: *Front End Of the Line* (FEOL) and *Back End Of the Line* (BEOL) structures. FEOL structures are designed to capture variations in the devices that are part of a circuit. FEOL structures are tested by carefully laying out sets of ring oscillators (ROs) whose inverters have been carefully laid out to enhance a specific source of variation. Any variations of these nature would be reflected in the overall output frequency of the RO. BEOL test structures on the other hand are structures that simulate common scenarios of interconnections within a chip. These structures must simulate parasitic capacitances such as fringing, coupling and plane capacitance. To do so, ring oscillators are carefully laid out to enhance all these variations, but exclusively one at a time in order to detect how this specific variation is affecting the output frequency of the circuit. Fig. 2 shows the representation of the entire chip. Note that each chip consists of 54 rows of ring oscillator and 6 rows of higher polysilicon density, for a total of 60 rows. The 54 rows of normal polysilicon density have 43 tiles each. There are 30 tiles among all 6 high polysilicon rows, for a total of 2,352 tiles per chip. A complete summary of the device positions can be found in Gonzalez [6].

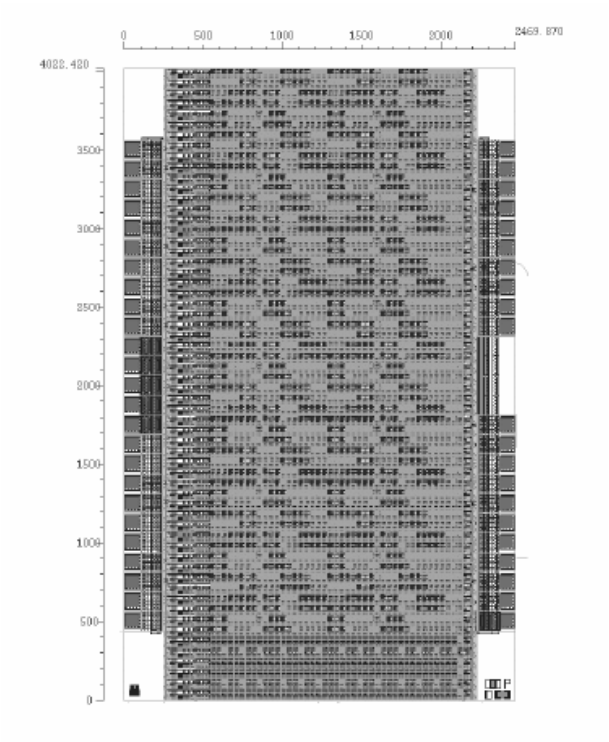

Fig. 2. Chip Layout [6]

In order to drawn any conclusions from the comparison between the parameter variations for the different devices, it is essential to investigate if there is any parameter correlations caused by common underlying variables due to some spatial dependence of a certain process. Wafer level and chip level spatial modeling are used to identify the trends. The details of the implementation of the spatial modeling are discussed in the following section.

III. Regression Fundamentals

This paper primarily focuses on standard analytical technique of linear regression. In the linear regression model, the dependent variable is assumed to be a linear function of one or more independent variables plus an error introduced to account for all other factors:

$$y_i = \beta_1 x_{i1} + ... + \beta_K x_{iK} + u_i \quad (1)$$

In the above *regression equation*, y_i is the *dependent variable*, x_{i1}, ..., x_{iK} are the *independent* or *explanatory variables*, and u_i is the *disturbance* or *error term*. The goal of regression analysis is to obtain estimates of the unknown parameters β_1, ..., β_K which indicate how a change in one of the independent variables affects the values taken by the dependent variable. The aim of regression is to make some predictive models, which can be used in future to estimate the dependent variable. The usual method of estimation for the regression model is ordinary least squares (OLS) [8]. Let b_1, ..., b_K denote the OLS estimates of β_1, ..., β_K. The predicted value of y_i is:

$$\hat{y}_i = b_1 x_{i1} + ... + b_K x_{iK} \quad (2)$$

The error in the OLS prediction of y_i, called the *residual*, is:

$$e_i = y_i - \hat{y}_i \quad (3)$$

The basic idea of ordinary least squares estimation is to choose estimates β_1, ..., β_K to minimize the sum of squared residuals:

$$\sum_1^n e_i^2 \quad (4)$$

It can be shown that:

$$b = (X'X)^{-1} X'y \quad (5)$$

where X is an n * k matrix with $(i,k)^{th}$ element x_{iK}, *y* is an n * k vector with typical element y_i, and *b* is a k * 1 vector with typical element b_K.

The least squares fitting procedure described below can be used for data analysis as a purely descriptive technique. However, the procedure has strong theoretical justification if a few assumptions are made about how the data are generated. One set of such assumptions, known as the Gauss-Markov assumptions that are sufficient to guarantee that ordinary regression estimates will have good properties are summarized [9]. The first assumption is that the errors u_i have an expected value of zero: $E(u_i) = 0$ This means that on average the errors balance out. Second assumption is that the independent variables are non-random. In an experiment, the values of the independent variable would be fixed by the experimenter and repeated samples could be drawn with the independent variables fixed at the same values in each sample. As a consequence of this assumption, the indenpendent variables will in fact be independent of the disturbance. For non-experimental work, this will need to be assumed directly along with the assumption that the independent variables have finite variances. Third, it assumes that the independent variables are linearly independent. That is, no independent variable can be expressed as a (non-zero) linear combination of the remaining independent variables. The failure of this assumption, known

as *multicollinearity*, clearly makes it infeasible to disentangle the effects of the supposedly independent variables. The fourth assumption is that the disturbances u_i are homoscedastic:

$$E(u_i^2)=\sigma^2 \quad (6)$$

This means that the variance of the disturbance is the same for each observation.

Fifthly, it assumes that the disturbances are not autocorrelated:

$$E(u_i u_j)=0 \quad (7)$$

This means disturbances associated with different observations are uncorrelated.

Regression models are fitted to the RO frequencies for different devices to test for within wafer level and within chip level spatial dependence. The center point for the x-y coordinates in the case of within wafer level regression models is defined to be at the center of the wafer. However, in the case of chip level linear regression models, the center point for the x-y coordinates are taken to be at the center of each individual chip. Goodness of fit, R^2, is calculated to investigate if the regression models are of a good fit.

IV. Results

Regression models are fitted to the RO frequencies for different devices to test for within wafer level and within chip level spatial dependence. The center point for the x-y coordinates in the case of within wafer level regression models is defined to be at the center of the wafer. However, in the case of chip level linear regression models, the center point for the x-y coordinates are taken to be at the center of each individual chip. Goodness of fit, R^2, is calculated to investigate if the regression models are of a good fit.

A. Wafer level spatial dependence analysis

The wafer level spatial dependence analysis is carried out in two parts. In the first part of the analysis, the average RO frequencies for all the device structures within each chip are averaged and data obtained for all the chips are analyzed using the regression model. In the second part, the average RO frequencies for all the devices of identical device structure within each chip are then calculated.

The chip mean frequencies by spatial location and the mean frequency for a best regression result for a device structure are plotted in Fig. 3 and 4 respectively. It is observed that there are no clear spatial wafer level trends in both Figs. 1 and 2. Regression model that uses parameters of x, y, xy, x^2 and y^2 yields R^2 value of 0.154 for the chip mean frequencies by spatial location. Regression models for all the 45 device structures also yield low R^2 value ranging from 0.04 to 0.22. Table 1 and 2 summarizes the model coefficients and the coefficients' significance at 95% confidence interval for the case of chip mean as well as the best regression fit for a certain device structure. From the two tables, it can be seen that the all model coefficients are not very significant at 95% confidence.

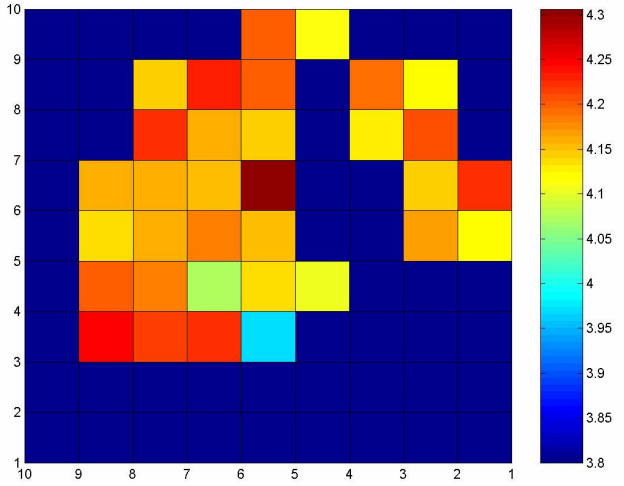

Fig. 3. Chip Mean Frequencies by Spatial Location

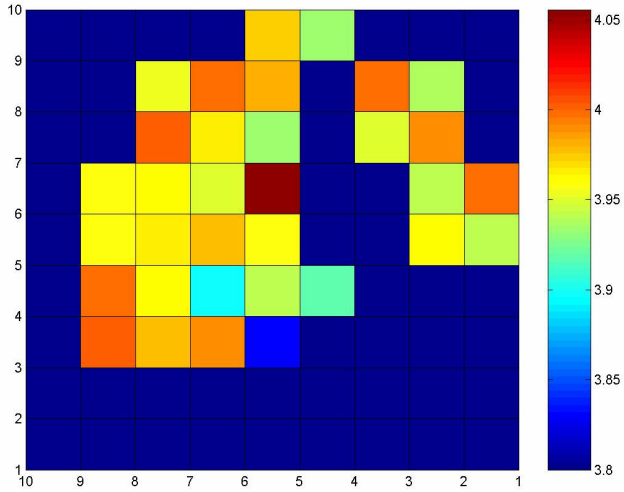

Fig. 4. Mean Frequencies for Plane Cap for ILD by Spatial Location

Table 1: Chip Mean Wafer Level Spatial modeling

	Coefficients	*Standard Error*	*t Stat*	*P-value*
Intercept	4081904.19	41430.55	98.52	0.00
X	-1098.54	717.22	-1.53	0.14
Y	2770.78	1824.28	1.52	0.14
XY	19.19	15.93	1.20	0.24
X^2	4.70	6.60	0.71	0.48
Y^2	-22.16	17.98	-1.23	0.23
R Square	0.15			

Table 2: Mean for Single Device Structure Wafer Level Spatial modeling

	Coefficients	*Standard Error*	*t Stat*	*P-value*
Intercept	3894742.24	25597.53	152.15	0.00
X	-765.26	443.13	-1.73	0.09
Y	2298.81	1127.12	2.04	0.05
XY	13.78	9.84	1.40	0.17
X^2	3.79	4.08	0.93	0.36
Y^2	-18.38	11.11	-1.65	0.11
R Square	0.22			

There can be several reasons for this observation; firstly there might not be any spatial correlation. Secondly, there can be a spatial correlation but not linear it might be non linear. Thirdly the data set might not be a good sample as it is missing values from other sides of wafer as shown in Fig.1.

B. Chip level spatial dependence analysis

After wafer level spatial analysis, chip level spatial dependence was carried out. As mentioned earlier, in the case of chip level linear regression models, the center point for the x-y coordinates are taken to be at the center of each individual chip. RO frequencies of individual device structure were regressed over x, y, xy, x^2 and y^2 to yield models. There are 45 device and 35 chips so it will yield (45x35=) 1575 models.

Table 3: R^2 value for different types of FEOL structure

	tile_ro1	tile_ro1_vert	tile_ro3	tile_ro3_vert
chip1	0.0616	0.1677	0.0721	0.1961
chip2	0.0203	0.1609	0.1405	0.1535
chip3	0.0554	0.1978	0.1912	0.2933
chip4	0.2159	0.5199	0.4211	0.4765
chip5	0.2123	0.6927	0.3881	0.8729
chip6	0.2036	0.7031	0.1802	0.7075
chip7	0.3741	0.7483	0.3982	0.7833
chip8	0.2256	0.7129	0.2280	0.7688
chip9	0.3077	0.7921	0.3160	0.8676
chip10	0.7901	0.9690	0.7649	0.9740
chip11	0.2404	0.6893	0.3672	0.8116
chip12	0.1837	0.6738	0.3239	0.6691
chip13	0.1471	0.5863	0.1709	0.7070
chip14	0.2238	0.6759	0.3722	0.7020
chip15	0.3020	0.7205	0.3707	0.7195
chip16	0.3492	0.7024	0.3666	0.7195
chip17	0.1039	0.4940	0.2663	0.7227
chip18	0.3269	0.7987	0.3358	0.7094
chip19	0.4950	0.8636	0.3328	0.9251
chip20	0.2263	0.5672	0.3735	0.5590
chip21	0.3377	0.8116	0.2747	0.8704
chip22	0.1861	0.6655	0.2656	0.6872
chip23	0.2210	0.7747	0.3213	0.7428
chip24	0.0940	0.5513	0.2472	0.4845
chip25	0.1932	0.7602	0.2481	0.7652
chip26	0.5376	0.8942	0.5743	0.8818
chip27	0.2634	0.7594	0.2376	0.7827
chip28	0.2066	0.6480	0.2760	0.6801
chip29	0.2232	0.7169	0.3443	0.7956
chip30	0.2992	0.1092	0.3512	0.7733
chip31	0.2408	0.6791	0.2933	0.7055
chip32	0.1110	0.6068	0.1487	0.6986
chip33	0.3080	0.5449	0.5677	0.7444
chip34	0.3341	0.7576	0.2894	0.7869
chip35	0.2513	0.5572	0.3607	0.6985

This work focuses on some interesting trends and devices, as it is not possible report such a large number of models. One of these interesting trends is observed in vertical and horizontal FEOL test structures. Horizontal and vertical test structures are designed to investigate the orientation dependence of structure. They primarily have the same architecture. There can be difference in their frequency attributed to mask scan bias or ion implantation effect.

Table 3 summarizes the R^2 value for two types of FEOL structure, which have both vertical and horizontal structure for all chips. The two FEOL structures are Canonical FEOL and 3x spacing FEOL. From this table it is evident that vertical structures have better fit as compared to horizontal. Note that there are also some chips (ie chip 1,2, …) that do not have any good R^2 value for all device structures measured.

Fig. 5 shows the spatial distribution for vertical Canonical FEOL for particular chip 19 and it can be observed that there is certainly a pattern to it. In given dataset, Chip 19 has the replication, which makes it more reliable and suitable candidate for spatial plots. R^2 value for this chip and device is 0.86 and coefficients are listed in Table 4.

Similarly, Fig. 6 shows the spatial distribution for horizontal Canonical FEOL for Chip 19. R^2 value for this regression was around 0.49 and its coefficients are also listed in Table 5.

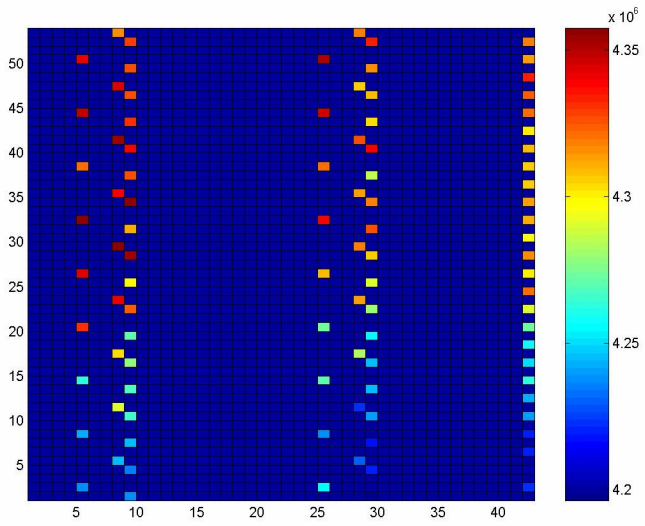

Fig. 5. RO1_vertical by Spatial Location

Table 4: Chip 19 RO1_Vertical Chip Level Spatial Modeling

	Coefficients	*Standard Error*	*t Stat*	*P-value*
Intercept	4315093.84	3206.79	1345.61	0.00
X	-14383.70	2093.34	-6.87	0.00
Y	25826.35	1682.54	15.35	0.00
XY	2080.24	1828.09	1.14	0.26
X^2	5003.95	3241.54	1.54	0.13
Y^2	-14144.47	1594.74	-8.87	0.00
R Square	0.86			

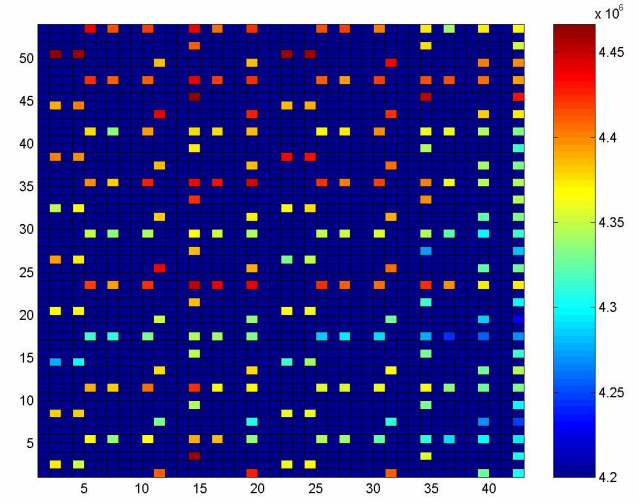

Fig. 6. RO1_Horizontal by Spatial Location

Table 5: Chip 19 RO1_Horizontal Chip Level Spatial Modeling

	Coefficients	*Standard Error*	*t Stat*	*P-value*
Intercept	4381108.63	4305.95	1017.45	0.00
X	-20520.43	3118.70	-6.58	0.00
Y	24800.59	2366.29	10.48	0.00
XY	4568.68	2840.55	1.61	0.11
X^2	-24246.59	4635.09	-5.23	0.00
Y^2	7640.08	2286.22	3.34	0.00
R Square	0.49			

From Table 4, is noted that for the case of the RO1 vertical device structure, the coefficients of x, y and y^2 in the regression model are very significant. The high R^2 value for the spatial model correlates well with the Fig. 5 that shows a clear trend that the measured device frequency increases diagonally from the bottom right to the top left hand corner of the chip.

From Table 5, is noted that for the case of the RO1 horizontal device structure, the coefficients of x, y, x^2 and y^2 in the regression model are significant. The relative low R^2 value for the spatial model correlates well with the Fig. 6 that shows that there exists only a slight trend that the measured device frequency increases diagonally from the bottom to the top of the chip.

V. Conclusion and Future Work

Wafer level spatial analysis shows that RO frequencies obtained from this dataset don't have linear spatial dependence on wafer level, as all R^2 values were low. It needs further investigation in terms of non-linear regression modeling to verify if there is any spatial model that exists in the system.

On the chip level, some interesting trends were observed such as some chips like Chip 1, 2, 3, which shows really low R^2 value for all device structures. This observation needs to be further investigated if there exists some potential process issues with these chips. On the other hand some device structures does have good R^2 value (>.0.6) for few chips such as FEOL horizontal.

The understanding of the interplay between the different levels of spatial dependence with the observed parameters is critical in order to establish the actual link between the variations in observed parameters to their various device parameters. The final objective is to isolate the variation in observed parameters due to various device parameters taking into account the generated spatial models

Acknowledgment

The authors would like to thank Karen Gonzalez for the useful discussions and providing the dataset for the analysis. The provision of a research grant from NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing and a research scholarship (L. W. Teo) and financial assistance to this project by the Singapore-MIT Alliance are gratefully acknowledged.

References

[1] D. Bartelink, "Statistical metrology-At the root of manufacturing control," *J. Vac. Sci. Technol. B*, vol. 12, pp. 2785-2794, July/Aug. 1994

[2] D. Boning and J. Chung, "Statistical metrology: Understanding spatial variation in semiconductor manufacturing," in *Microelectronic Manufacturing Yield, Reliability, and Failure Analysis II: SPIE 1996 Symp. On Microelectronic Manufacturing*, Oct. 1996, Austin, TX.

[3] J. Kibarian and A. Strojwas, "Using the spatial information to analyze correlations between test structure data," *IEEE Trans. Semicond. Manufact.*, vol. 4, pp. 219-225, Aug. 1991

[4] B. E. Stine, D. Boning and E.C. Chung, "Analysis and decomposition of spatial variation in integrated circuit Processes and Deivces," *IEEE Trans. Semicond. Manufact.*, vol .10. no. 1, Fed, pp. 24-41, Feb. 1997.

[5] J. S. Panganiban, "A ring oscillator based variation test chip," Master dissertation, Dept. Elect. Eng. And Comp. Sci., Massachusetts Institute of Technology, Cambridge, MA, 2002.

[6] K. M. Gonzalez, "Extraction of variation sources due to layout practices," Master dissertation, Dept. Elect. Eng. And Comp. Sci., Massachusetts Institute of Technology, Cambridge, MA, 2002.

[7] Available: http://www.mosis.org/

[8] G. E. P. Box, W. G. Hunter, J. S. Hunter, "Statistics for Experimenters," Wiley Series, New York, 1978.

[9] Available: www.hss.caltech.edu/~jad/sst/html/regression.html