Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.776
High Speed Communication Circuits
Spring 2005

Homework #5: Narrowband LNA and VCO Design
Passed Out: March 29, 2005 Due: April 5, 2005

Reading: Chapters 11 and 16 of Thomas H. Lee's first edition book OR Chapters 12 and 17 of Thomas H. Lee's second edition book.

---

1. This problem will focus on design of the LNA shown in Figure 1. In the figure, L_{deg} (L_s) is assumed to have infinite Q, but inductors L_g and L_d have associated resistances due to their finite Q (i.e., the values of R_{pg} and R_{pd} are set by the Q and inductance value of L_g and L_d, respectively). Assume the following

   - Design of the LNA should be focused on its performance at frequency w_o = (2π)1.8 GHz
   - If an external inductor is used for L_g, its Q is 40. For integrated inductors, assume the Q to be 7 (other than for L_{deg}).
   - The LNA input impedance, Z_{in}, must be designed to match that of the source resistance of 50 Ohms at frequency w_o (Note: assume C_{big} is a short at frequency w_o)
   - The power dissipation of the core amplifier must be no greater than 20 mW. (Ignore the bias circuitry here)
   - All transistor devices are the same size and have length L=0.18 μm
   - The influence of the cascode device M_2 can be ignored for noise figure and gain calculations.
   - Ignore C_{gd}, C_{db}, r_o, and backgate effects for all transistors.
   - Ignore the noise contribution of transistors M_2 and M_3 and the 5 kΩ bias resistor.
   - Assume the following process parameters
     - c = -j0.55
     - $\gamma = 3$
     - $\delta = 6$

- $g_m/g_{do} = 0.7$
- $w_t = (2\pi)43$ GHz
- $I_{den} = 100\ \mu$A/μm
- $g_m = \frac{W}{1.8}$ 0.8 mS, where W is transistor width in microns
- V_{dd}= 1.8 V

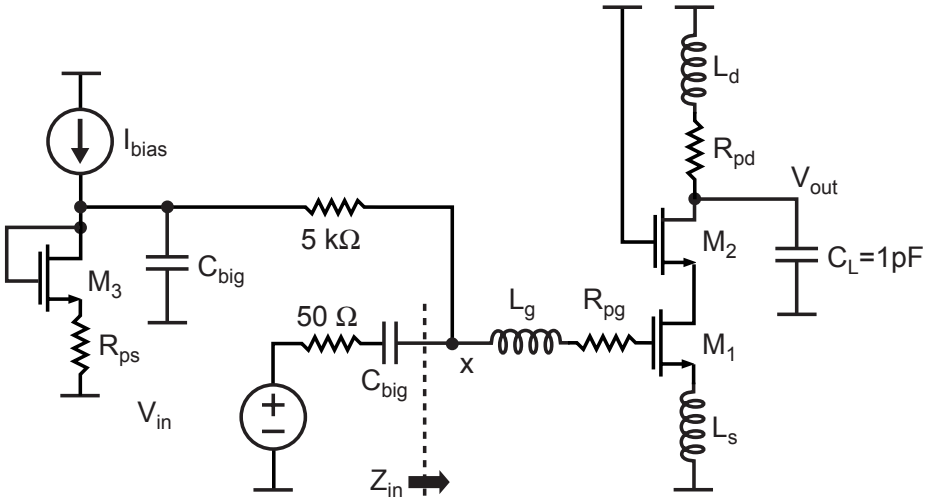

Figure 1: Narrowband LNA.

(a) Design the amplifier to achieve the minimum noise figure given the conditions stated above. State the resulting noise figure (at w_o), I_{bias}, transistor widths, component values, and gain (at w_o) for the amplifier. For intermediate calculations, determine η, χ_d, and Z_{gsw}.

(b) If power is a free variable (current density is still fixed at 100μA/μm), is there an optimum I_{bias} (or W) to minimize the noise figure? If so, state the noise figure (at w_o), Ibias, transistor widths, component values and gain (at w_0) for the new design.

(c) How does the noise figure change for part (a) if c = -0? (a numerical answer is required here)

(d) How does the noise figure change for part (a) if c = -j1? (a numerical answer is required here)

2. The following is based on Problem 2 in Chapter 16 of Thomas Lee's first edition book. Here we examine the Colpitts oscillator shown in Figure 2. Use the 0.18u Spectre model file provided on MIT server in the file /mit/6.776/Models/0.18u/cmos018.scs for your MOS model.

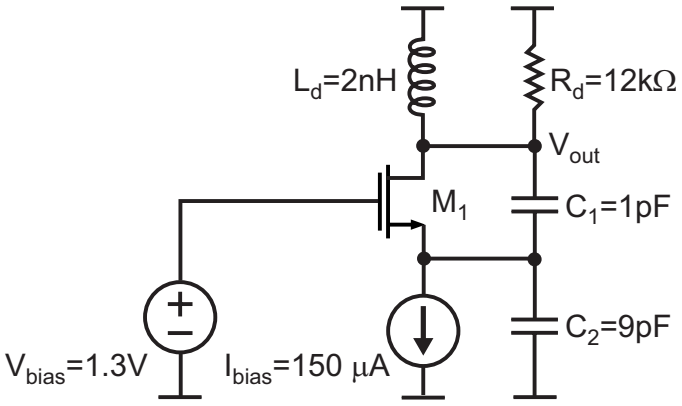

Figure 2: CMOS Colpitts oscillator.

(a) Neglecting transistor capacitances and r_o, calculate the minimum W/L ratio necessary for a startup gain of 2 under the assumption that the device obeys the square law for its V_{gs} to I_d curve. What should L be set to? Explain.

(b) Why not set the startup gain to a value slightly higher than 1 rather than a value of 2 as assumed in part (a)? Explain the tradeoffs (i.e., benefits and negatives) of doing so.

(c) Given the same conditions as part (a), find the minimum W using Spectre. Use the L value previously selected in (a).

(d) Enter in the full circuit schematic in Cadence, and simulate in Spectre. Create a time-domain plot of the oscillator output that displays its startup transient and steady-state oscillation. If you need to change circuit component values to achieve steady-state oscillation, then explain why the changes are needed.

(e) Given the circuit you end up with in part (d), create a phase noise plot in Spectre of the VCO output with frequency offset range spanning 1kHz to 30 MHz. Note that the Spectre tutorial by Albert Jerng describes how to produce this plot.

(f) Repeat parts (d) and (e) with R_d changed from 12 kΩ to 24 kΩ.