Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.776
High Speed Communication Circuits
Spring 2005

Homework #4: Narrowband Amplifiers and Noise
Passed Out: March 10, 2005 Due: March 17, 2005

Reading: First edition of T.H. Lee's book: Chapter 10 and pages 272-284 & 295-300 OR Second edition of T.H. Lee's book: Chapter 11 and pages 364-380 & 390-397.

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1. This problem will focus on the design of the narrowband amplifier shown in Figure 1. Assume that all devices are the same size with width of 80 microns and length of 0.18 microns. For all hand calculations, ignore C_{gd}, r_o, backgate effects, and overlap for all transistors.

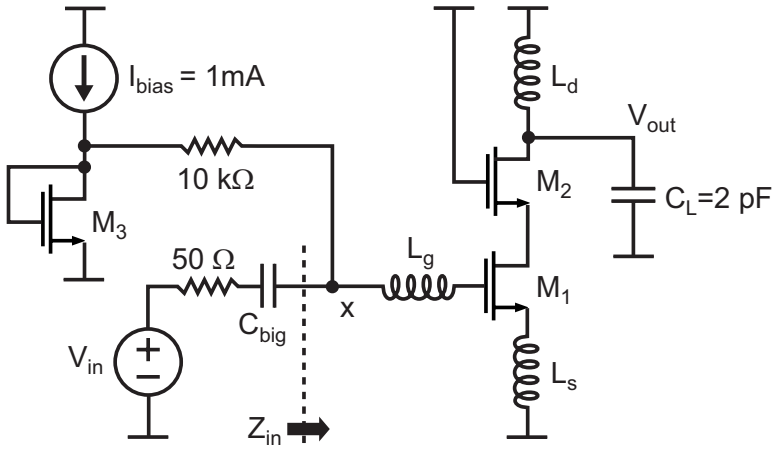

Figure 1: A high speed, tuned cascode amplifier.

(a) Compute C_{gs} and g_m for all the transistors at the operating point set by the bias configuration shown in the figure. Be sure to determine these parameters "by hand" based on the transistor parameters contained in the 0.18u Spectre model file provided on MIT server in the file /mit/6.776/Models/0.18u/cmos018.scs. For all parts to follow, use C_{gs} and g_m from Spectre and also include the appropriate C_{db}.

(b) Given that the Q of all of the inductors at 5 GHz is 6, determine L_s, L_g, and L_d to achieve 50 Ohm input impedance (Z_{in}) and maximum gain (V_{out}/V_{in}) at 5 GHz. Use a simple inductor model of a resistor in series with an inductor. State the maximum gain that you achieved.

(c) Repeat part (b) given that the Q of all of the inductors at 5 GHz is 30. How does the maximum gain change?

(d) Build the two circuits from (b) and (c) in Cadence Composer on MIT server and use Spectre to plot Z_{in} (real and imaginary parts) and the amplifier gain (V_{out}/V_{in}) over the frequency range of 1 GHz to 20 GHz.

(e) Using Spectre, plot $|S_{11}|$ and $|S_{21}|$ over the frequency range of 1 GHz to 20 GHz for both circuits in (d). For these exercises, assume that the input of the two-port is node x, and that the output is V_{out}.

2. The following is based on Problem 5 in Chapter 11 of Thomas Lee's first edition book. Consider the resistively shunted amplifier shown in Figure 2. V_{dd}=1.8 volts, $I_{bias} = 400\mu$A, and R_1 is chosen such that all transistors are in saturation.

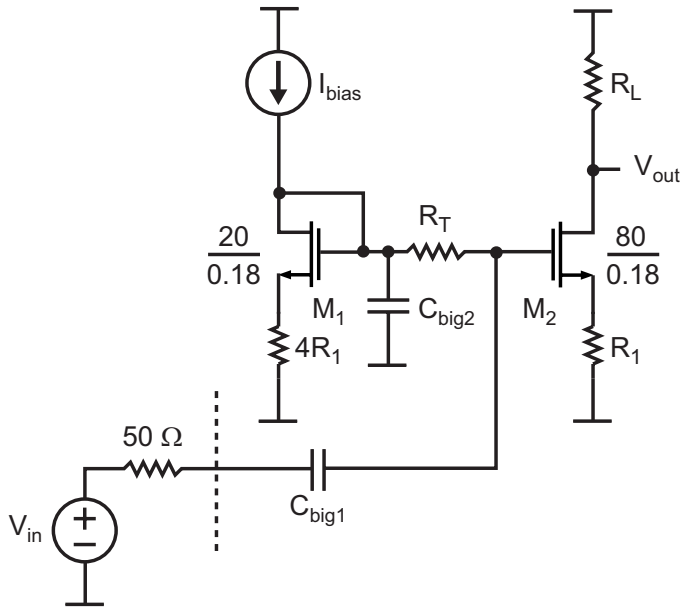

Figure 2: Amplifier with resistive input termination.

(a) Assuming $R_L = 500\ \Omega$, all transistors are in saturation and neglecting the back-gate effect:

i. What voltage is V_{out} biased at? How much current flows through M_2?

ii. Using Spectre, find g_m and C_{gs} for M_2 with 0.18 μm Spectre model file provided on MIT server in the file /mit/6.776/Models/0.18u/cmos018.scs.

(b) Assuming that C_{big1} and C_{big2} are short circuits at the frequencies of interest, redraw a simplified version Figure 2 for calculating the noise figure of the amplifier.

(c) Given the assumption in part (b), does the bias transistor M_1 impact the noise figure of the amplifier?

(d) Derive an expression for the noise figure (factor) of the amplifier. Assume that all transistors are in saturation, and ignore the impact of gate noise, C_{gd}, r_o, and

source/drain capacitances in M_2. Also assume for M_2 that

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f, \quad g_m/C_{gs} = w_T,$$

where the excess noise factor $\gamma = 3$ and $\alpha = 0.5$.

(e) Based on your expression in part (d):

i. Is the noise figure a function of frequency? If so, is the noise performance of the amplifier better at high or low frequencies?

ii. Is the noise figure of the amplifier minimized for $R_T \ll 50\Omega$, $R_T = 50\Omega$, or $R_T \gg 50\Omega$?

iii. How does the noise figure change as a function of $\frac{R_L}{R_1}$? Explore the two cases where $R_1 = 0$ and where $R_L = R_1$ and explain the result.

iv. Assuming that $\frac{w_T}{w} = 10$, what is the minimum noise figure that can be achieved when $R_1 = 250\Omega$? With $R_1 = 50\Omega$? (Set R_T to minimize the noise figure.)

v. For the same two cases, what is the noise figure for $R_T = 50\Omega$ with $\frac{w_T}{w} = 10$?

(f) Rederive the expression for noise figure (factor) of the amplifier under the same conditions as in part (d) except that you should now include the impact of gate noise and assume that $R_1 = 0$. Assume that the gate noise is described as:

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f, \quad \text{where } g_g = w^2 C_{gs}^2/(5 * g_{do}),$$

where the gate noise coefficient $\delta = 6$. Also assume that gate noise is correlated with drain noise as:

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd^2}}}} = -j0.55$$

(g) Is the noise figure a function of frequency? If so, is the noise performance of the amplifier better at high or low frequencies?

(h) What is the noise figure for $R_T = 50\Omega$, $\frac{w_T}{w} = 10$?

3. Now consider the resistively shunted amplifier employing a cascode transistor as shown in Figure 3. For the questions below, assume that all transistors are in saturation and $\omega \ll \omega_T$. Ignore the impact of gate noise, C_{gd}, r_o, and source/drain capacitances in M_2 and M_3. Also assume for M_2 and M_3 that

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f, \quad g_m/C_{gs} = w_T,$$

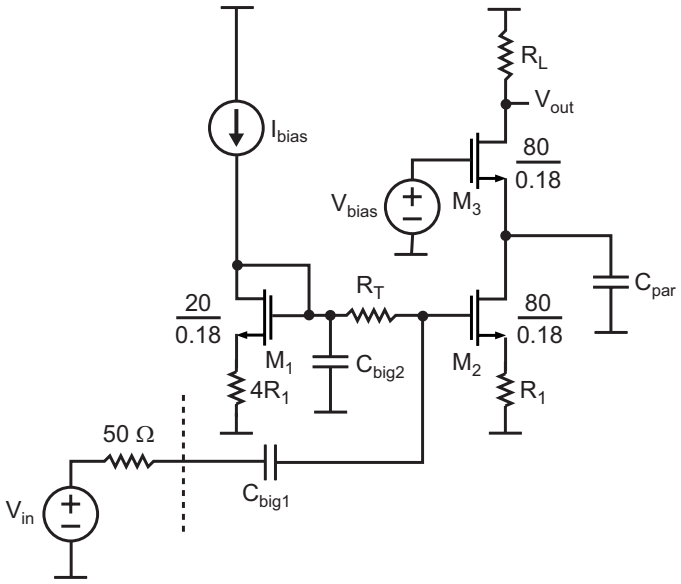

Figure 3: Cascoded amplifier with resistive input termination.

(a) From an intuitive perspective, what is the impact of M_3 on the overall noise figure of the amplifier if $C_{par} = 0$? Justify your answer.

(b) Also from an intuitive perspective, how does C_{par} impact the overall noise figure as its value is increased above zero? Justify your answer.