Massachusetts Institute of Technology

Department of Electrical Engineering and Computer Science

6.111 - Introductory Digital Systems Laboratory

Quiz 1 September 27, 2002

1	.....(30)
2	.....(40)
3	.....(30)
TOTAL	.....(100)

SOLUTION

Indicate Your Section

( ) James 12 PM
( ) Jennifer 1 PM
( ) Neira 3 PM

This quiz is **Closed Book:** One handwritten "crib" sheet is allowed.

Put your name on all sheets and indicate your section on this page.

Write all your answers directly on the quiz.

Show all of your work.

You are not required to use a logic template, but you must **make sure your answers are legible**.

Problem 1: Finger Exercises

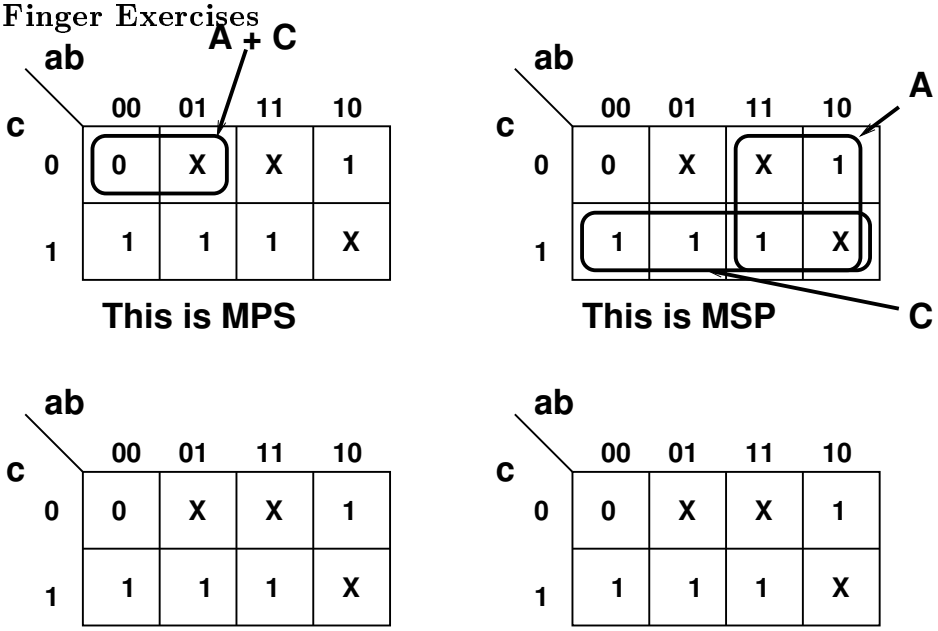

Figure 1: Karnaugh Maps of a logical function

Figure 1 shows four copies of the Karnaugh map of some logic function.

1. Show the groupings that correspond with the MINIMAL product of sums for this function. Use one of the k-maps and indicate which one is MPS.

2. What is the expression for the MPS?

   F = C + A

3. Show the groupings that correspond with the MINIMAL sum of products for this function. Use another of the k-maps and indicate which one is MSP.

4. What is the expression for the MSP?

   F = A + C

5. Do either of these logical functions exhibit a static hazard? If so, which one?

   Answer: No, neither has a static hazard

6. Are the logical functions equal?

   Answer: Yes

Problem 2: Finite State Machines

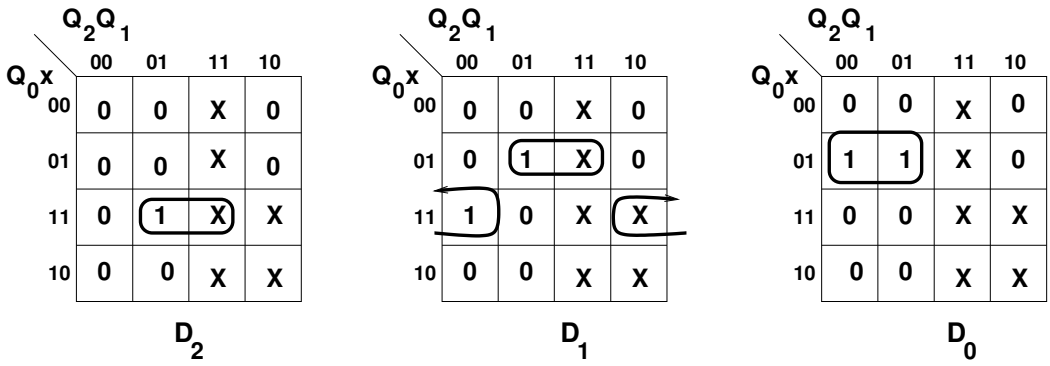

Figure 2: Karnaugh Maps for FSM

You have been hired by Itsy-Bitsy Machine Company and your first job is to resurrect a finite state machine that was designed by a junior engineer who is no longer with the company. Seems as if this person was very sloppy and the only information you can find is a single page of paper containing the Karnaugh Maps shown in Figure 2. There are obviously three state variables and it appears there is one input (x). Since the states 101, 110 and 111 have don't cares in them, it appears that only states 0 through 4 (000, 001, 010, 011 and 100) are of interest.

1. What are the MINIMAL logical expressions for each of the state variable inputs (that is, the input to the flip-flop that will hold the state). Assume the D-type flip flops are to be used.

   $D_2 = Q_1 * Q_0 * x$

   $D_1 = Q_1 * \overline{Q}_0 * x + \overline{Q}_1 * Q_0 * x$

   $D_0 = \overline{Q}_2 * \overline{Q}_0 * x$

2. On the state transition diagram shown in Figure 3, show the actual transitions exhibited by this machine, as influenced by the input x.

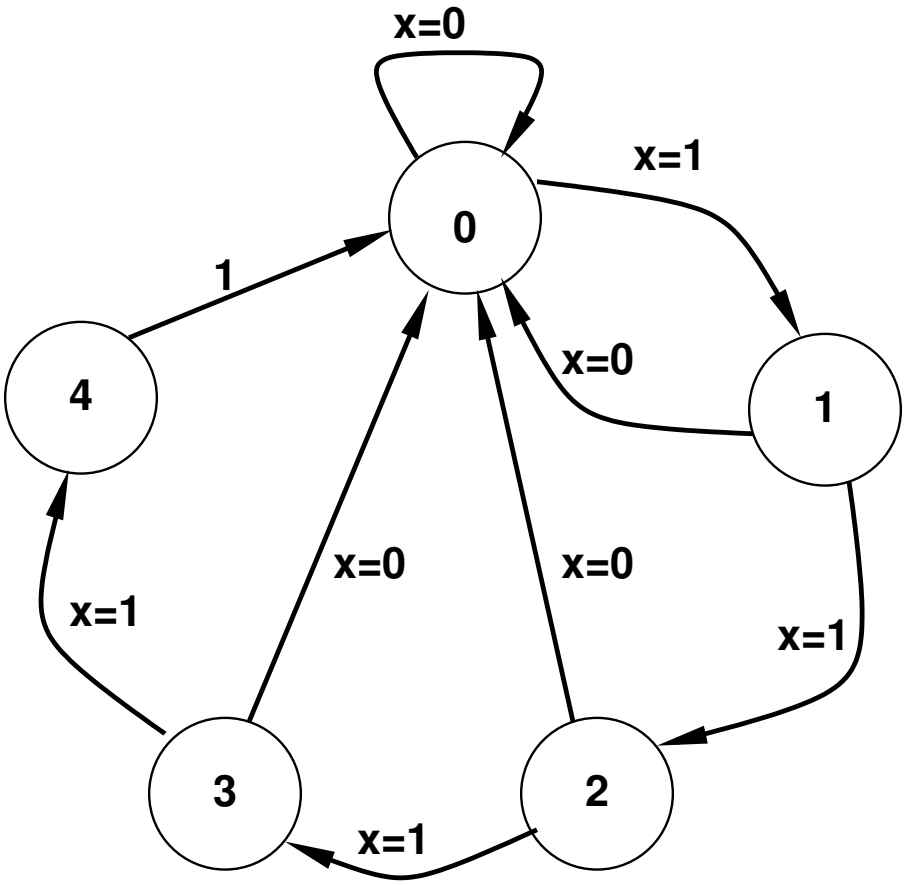

Figure 3: IBM Finite State Machine

Problem 3: Timing A logical circuit with two flip-flops is shown in Figure 4. Assume the following timing parameters:

1. Gate Delay 20 nS
2. FF Clock to Q Delay 10 nS
3. FF Asynchronous Input to Q 5 nS

These flip-flops have *asynchronous* clear inputs.

On the timing diagram of Figure 5, show the operation of the circuit. Assume that at the beginning both flip-flops have Q=0.

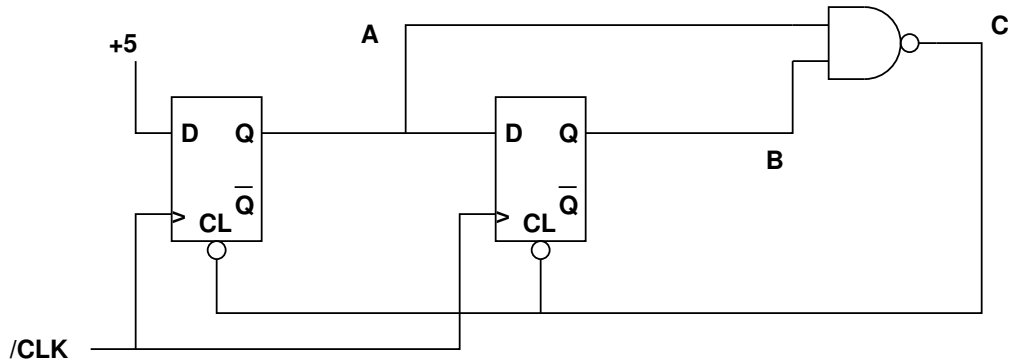

Figure 4: Funny Circuit

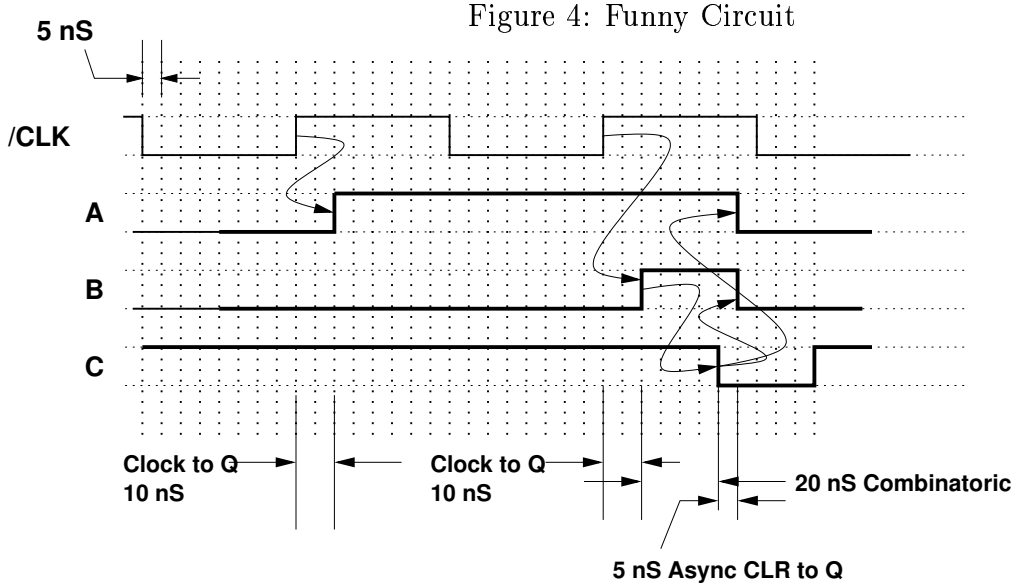

Figure 5: Timing Diagram for Problem 3