6.012 - Microelectronic Devices and Circuits

Lecture 21 - Diff-Amp Anal. II: Output Stages - Outline

- **Announcements**
  - **DP:** Get help before the Thanksgiving break. It's due Friday, Dec. 4
  - **On Stellar:** Write-up on the cascode connection posted under Lec. 21
    Lee Load and Current Mirror Load write-ups posted under Lec. 20.
- **Review - Non-linear and Active Loads**
  - **Maximum gain:** $A_{v,max} \propto V_{A,eff}/(V_{GS}-V_T)_{min}$ for MOS; $\propto V_{A,eff}/V_{themal}$ for BJT
  - **Lee Load, Current Mirror:** foils on analysis of CM in DP
- **Specialty Stages - useful transistor pairings**
  - **Source-coupled pairs**
  - **The Marvelous Cascode:** Postponed until Lecture 22
  - **Push-pull or Totem Pole output stages**
- **Performance metrics - continuing down the list**
  - **Output resistance:** Driving a load
  - **DC off-set on output:** High impedance nodes; feedback connections
  - **Power dissipation:** Add up currents from voltage supplies

Achieving the maximum gain: Comparing linear resistors, current sources, and active loads

Maximum Gains

	MOSFET (SI) (w. and w.o. velocity sat.)	Bipolar-like (Sub-V_T MOS and BJT)
Linear resistor loads	$\leq \dfrac{2\left[I_D R_{SL}\right]_{\max}}{\left[v_{GS}-V_T\right]_{\min}}$	$\leq \dfrac{\left[I_C R_{SL}\right]_{\max}}{n\,V_t}$
Current source loads	$\leq \dfrac{2V_{A,eff}}{\left[v_{GS}-V_T\right]_{\min}}$	$\leq \dfrac{V_{A,eff}}{n\,V_t}$
Active loads		
Difference mode	$\propto \dfrac{2V_{A,eff}}{\left[v_{GS}-V_T\right]_{\min}}$	$\propto \dfrac{V_{A,eff}}{n\,V_t}$
Common mode	$\propto \dfrac{\left[v_{GS}-V_T\right]_{\min}}{2V_{A,bias}}$	$\propto \dfrac{n\,V_t}{V_{A,bias}}$

Observations/Comments:

- Non-linear (current source) loads typically yield much higher gain than linear resistors, i.e. $V_{A,eff} >> [I_D R_{SL}]_{max}$.
- The bias point is not as important to BJT-type stage gain.
- An SI MOSFET should be biased just above threshold for highest gain.
- For active loads what increases A_{vd}, decreases A_{vc}.
- Making L larger increases V_A proportionately, but at the cost of speed.

Achieving the maximum gain: $(v_{GS}-V_T)_{min}$ = ?

For SI-MOSFETs, maximizing the voltage gain (A_v or A_{vd}) requires minimizing ($V_{GS}-V_T$). What is the limit?

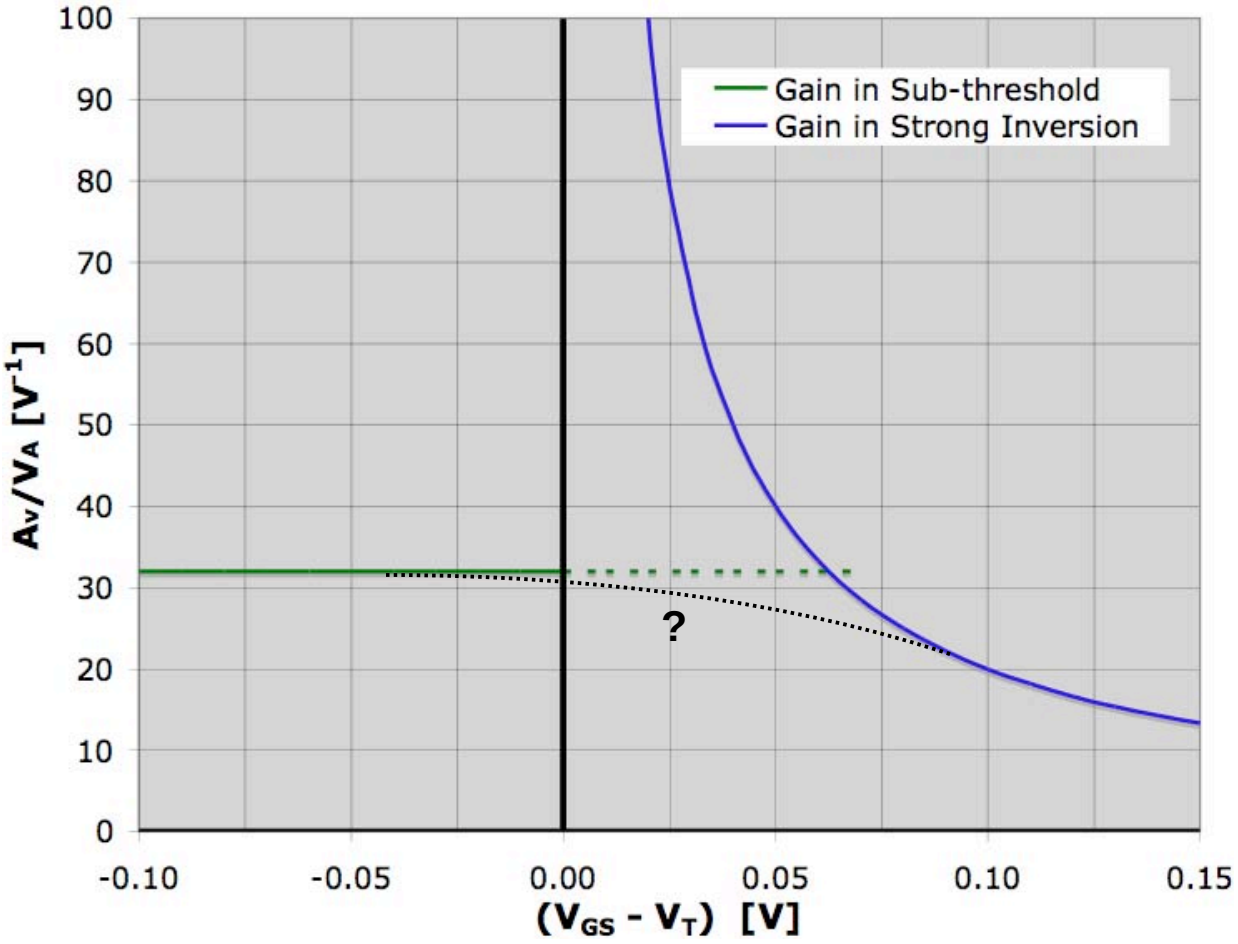
Sub-threshold:

$$\left|\frac{A_v}{V_A}\right| = \frac{1}{n\,V_t}$$

Strong inversion:

$$\left|\frac{A_v}{V_A}\right| = \frac{2}{(V_{GS}-V_T)}$$

A_v/V_A is a smooth curve, so clearly $(V_{GS}-V_T)_{min} > 2nV_t$.

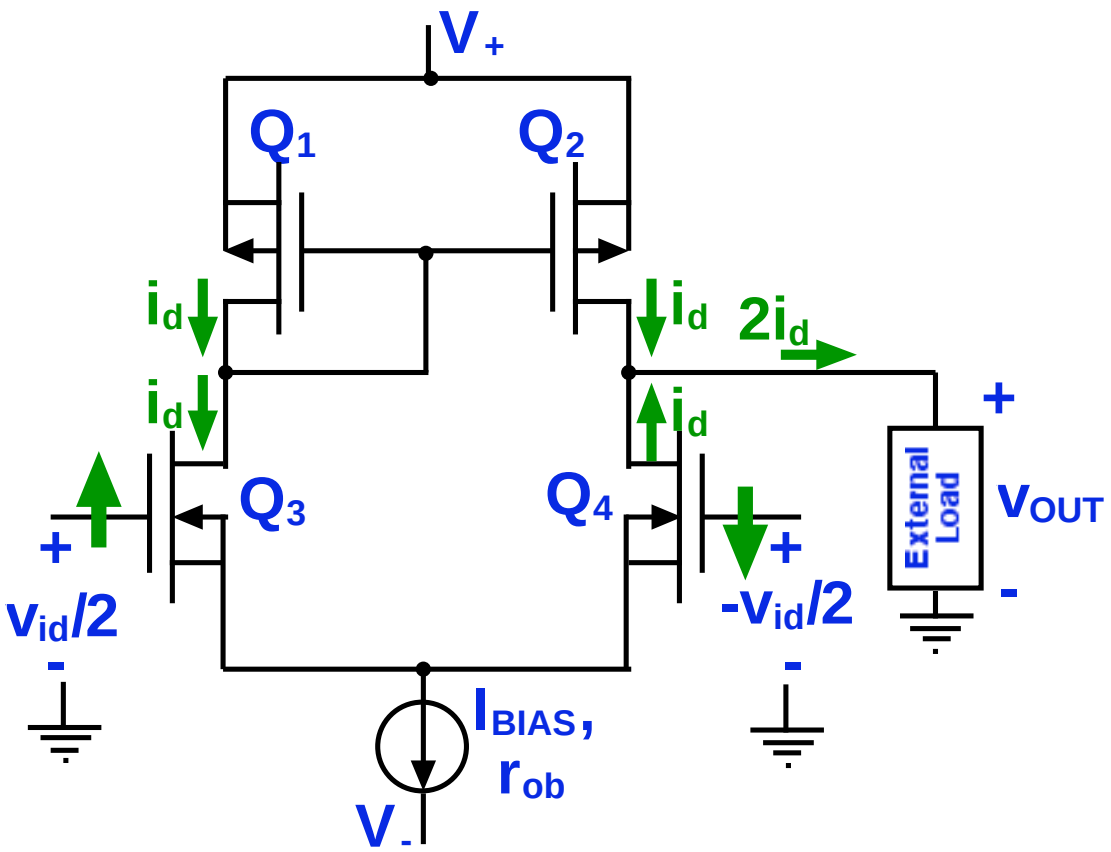


Note: n = 1.25 was assumed.

Active Loads: The current mirror load

Large differential-mode gain, small common-mode gain.
Also provides high gain conversion from double-ended to single-ended output.

The circuit is no longer symmetrical, so half-circuit techniques can not be applied. The full analysis is found in the course text. We find:



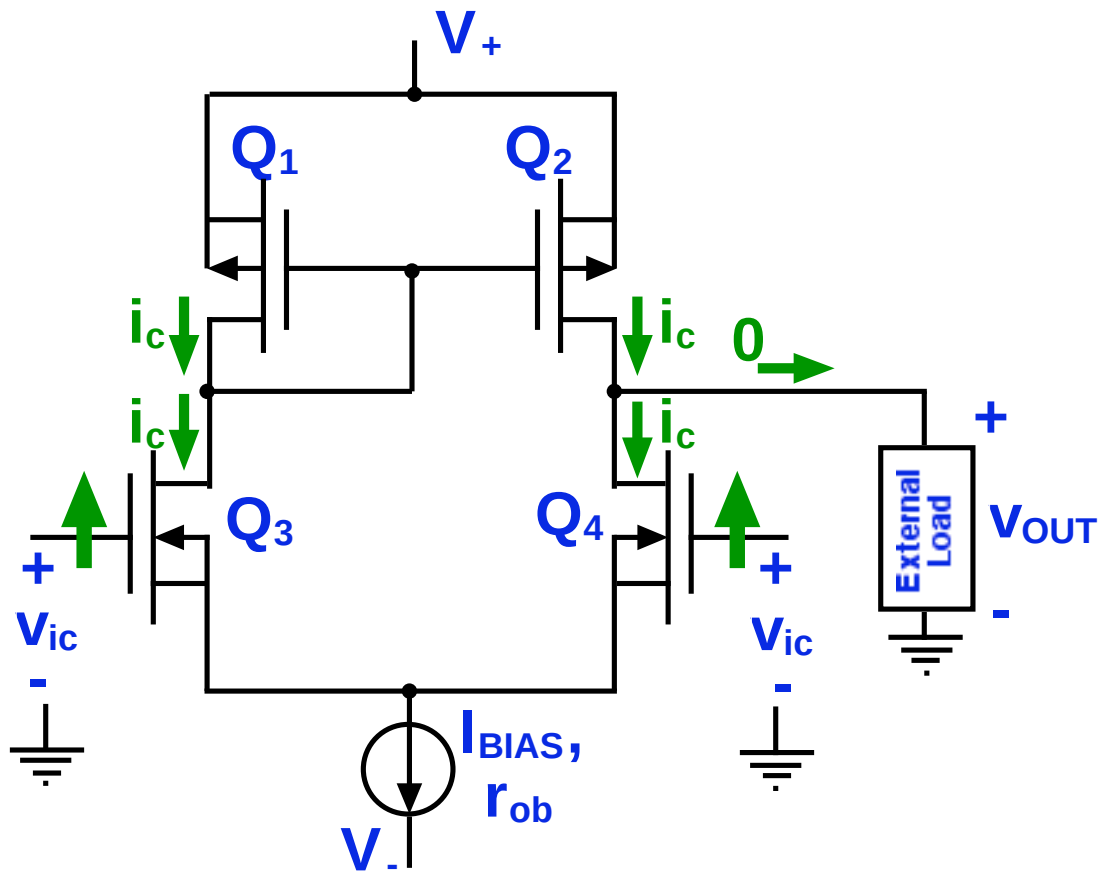
Difference-mode inputs

$$v_{out,d} = \frac{2g_{m3}}{(g_{o2} + g_{o4} + g_{el})} v_{id}/2$$

Active Loads: The current mirror load, cont.

Common-mode inputs

$$v_{out,c} = \frac{g_{ob}}{2g_{m2}} v_{ic}$$



With both inputs:

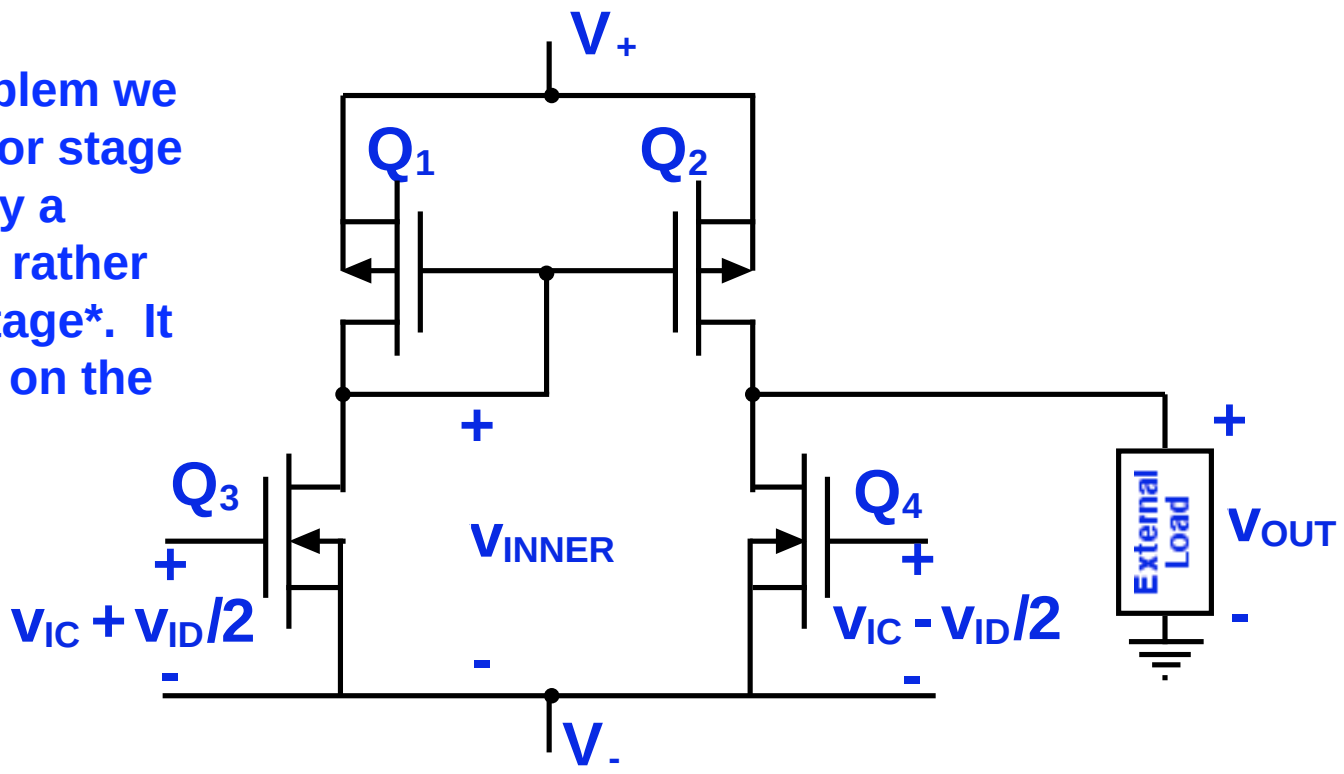
$$v_{out} = \frac{2g_{m3}}{(g_{o2} + g_{o4} + g_{el})} \frac{(v_{in1} - v_{in2})}{2} - \frac{g_{ob}}{2g_{m2}} \frac{(v_{in1} + v_{in2})}{2}$$

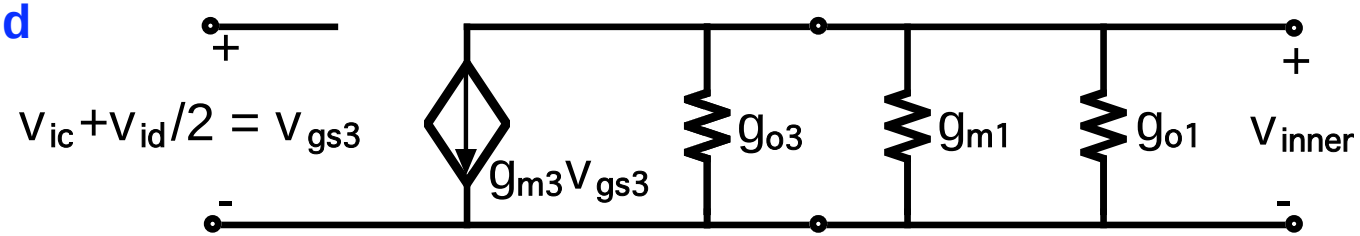
Note: In D.P. the output goes to the gate of a BJT; g_{el} matters.

Active Loads: A current mirror load variant (D.P. version)

In the design problem we have a current mirror stage that is not biased by a current source, but rather by the preceding stage*. It thus looks like that on the right.

We can do an LEC analysis of this circuit fairly easily. We start with the LEC for the left side and find v_{inner}:





LEC for the left side

* Notice that it is possible to make the bias currents in the two legs of the mirror (Q_1/Q_3 and Q_2/Q_4) different by making the transistors widths different.

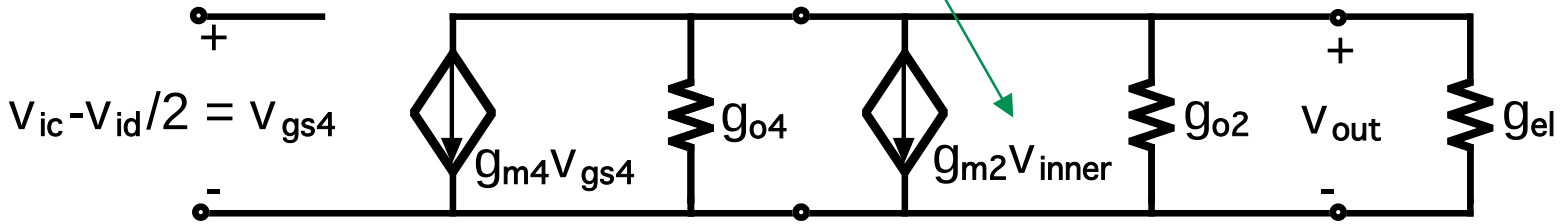
Active Loads: A current mirror load variant, cont.

The left side LEC gives:

$$v_{inner} = \frac{-g_{m3}}{(g_{o3} + g_{o1} + g_{m1})}\left(v_{ic} + \frac{v_{id}}{2}\right)$$

Note: Make $g_{m1} = g_{m3}$, $g_{m2} = g_{m4}$, $g_{o1} = g_{o3}$, and $g_{o2} = g_{o4}$.

Next we analyze the right side LEC:



LEC for the right side

This then gives us v_{out}:

$$v_{out} = \frac{-g_{m4}}{(g_{o4} + g_{o2} + g_{el})}\left(v_{ic} - \frac{v_{id}}{2}\right) + \frac{-g_{m2}}{(g_{o4} + g_{o2} + g_{el})}\frac{-g_{m3}}{(g_{o3} + g_{o1} + g_{m1})}\left(v_{ic} + \frac{v_{id}}{2}\right)$$

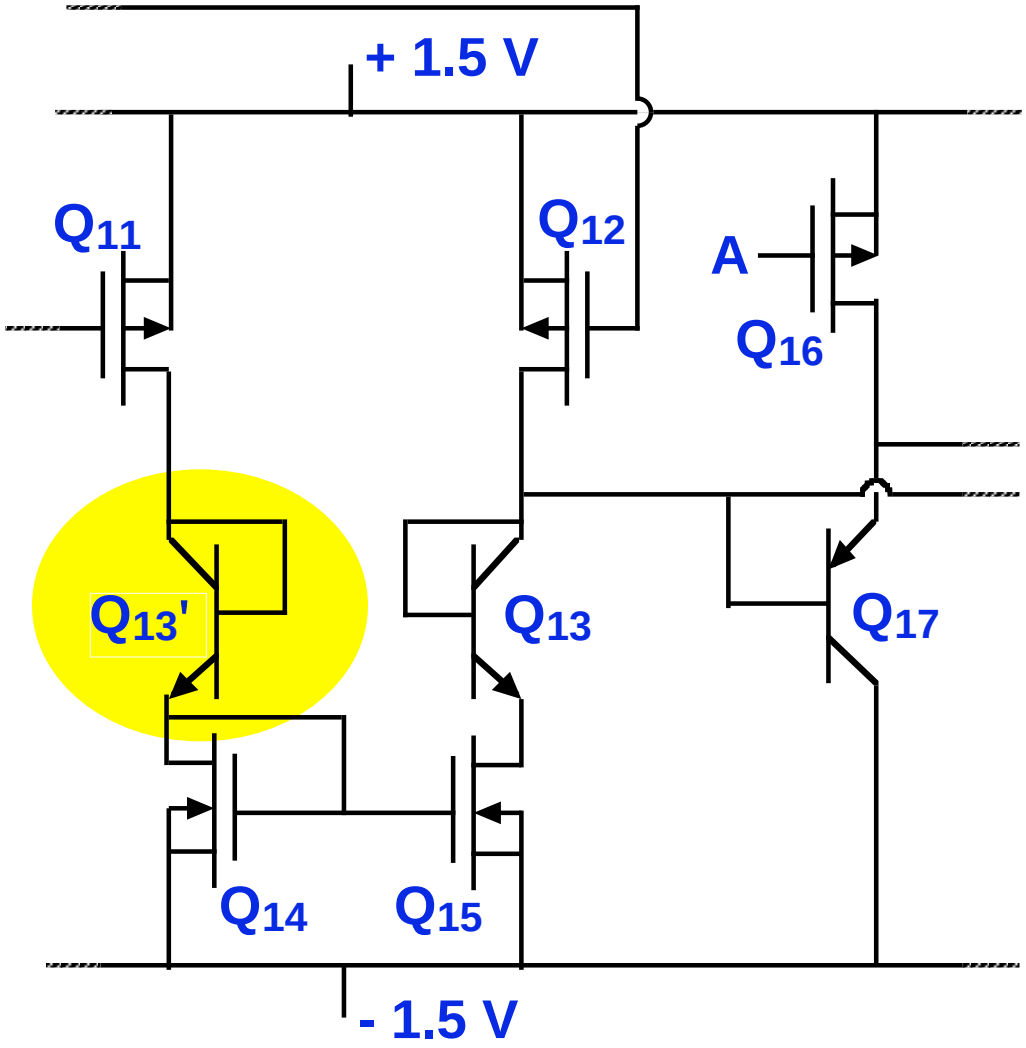
$$= \frac{g_{m4}}{(g_{o4} + g_{o2} + g_{el})}\frac{v_{id}}{2}\left[1 + \frac{g_{m3}}{(g_{o3} + g_{o1} + g_{m1})}\right] - \frac{g_{m4}}{(g_{o4} + g_{o2} + g_{el})}v_{ic}\left[1 - \frac{g_{m3}}{(g_{o3} + g_{o1} + g_{m1})}\right]$$

$$\approx \underbrace{\frac{2g_{m4}}{(2g_{o4} + g_{el})}}_{A_{vd}}\frac{(v_{in1} - v_{in2})}{2} - \underbrace{\frac{g_{m4}}{(2g_{o4} + g_{el})}\frac{2g_{o1}}{g_{m1}}}_{A_{vc} \approx 1}\frac{(v_{in1} + v_{in2})}{2}$$

Note: The difference-mode response is unchanged, but now $A_{vc} \approx 1$, not << 1.

An aside: More on the design problem CM stage

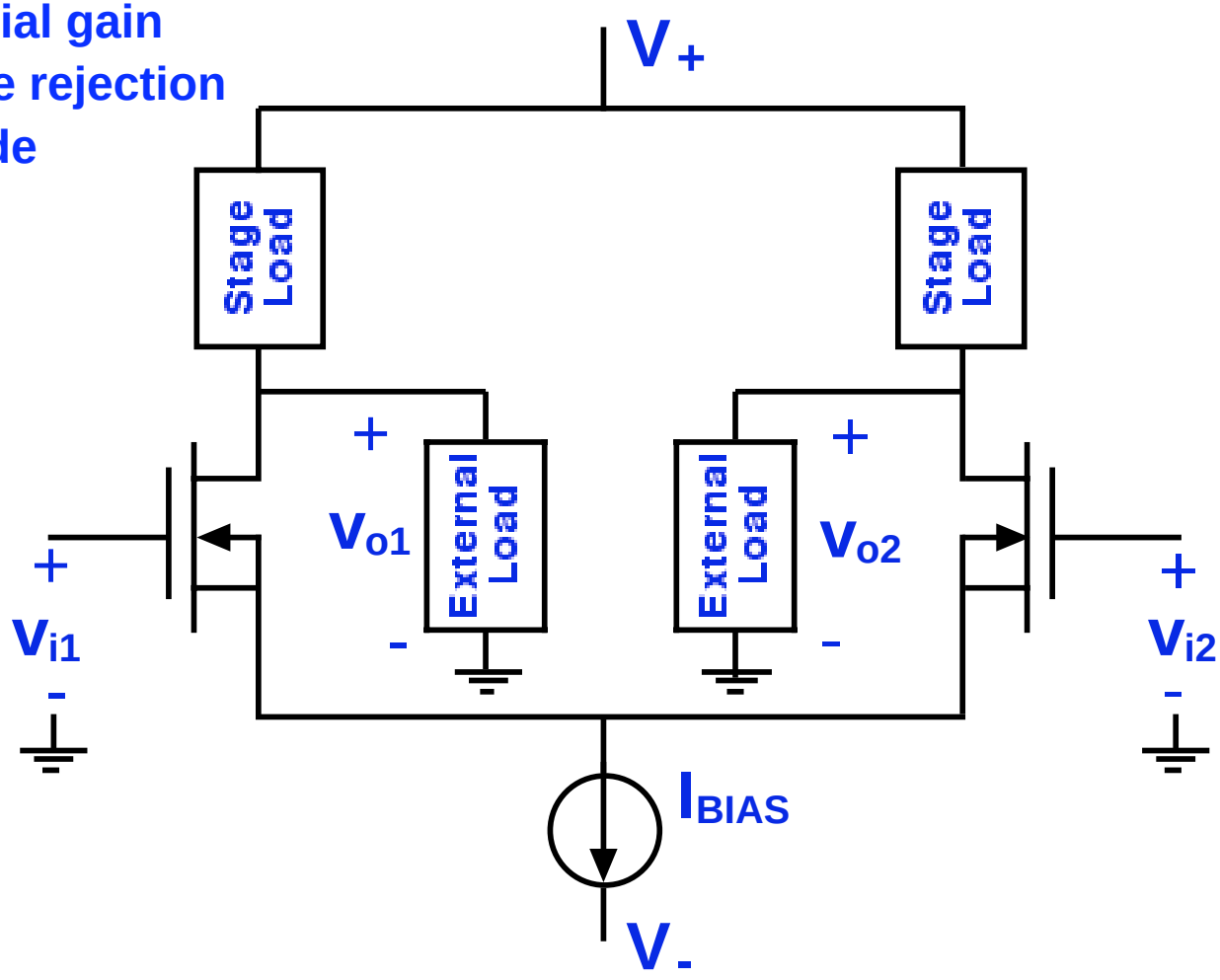
Transistor Q_{13} does not have a companion on the left side of the second DP gain stage (the Current Mirror). If we ignore the Early effect for the large signal biasing analysis, as you have been told to do, this is fine. However, strictly speaking, it is best to maintain symmetry and thus you should add a companion transistor, $Q_{13'}$, as shown to the right.



Specialty Pairings: The Source-coupled Pair

Two coupled common-source stages

- Large differential gain
- Common-mode rejection
- Easy to cascade
- Easy to bias

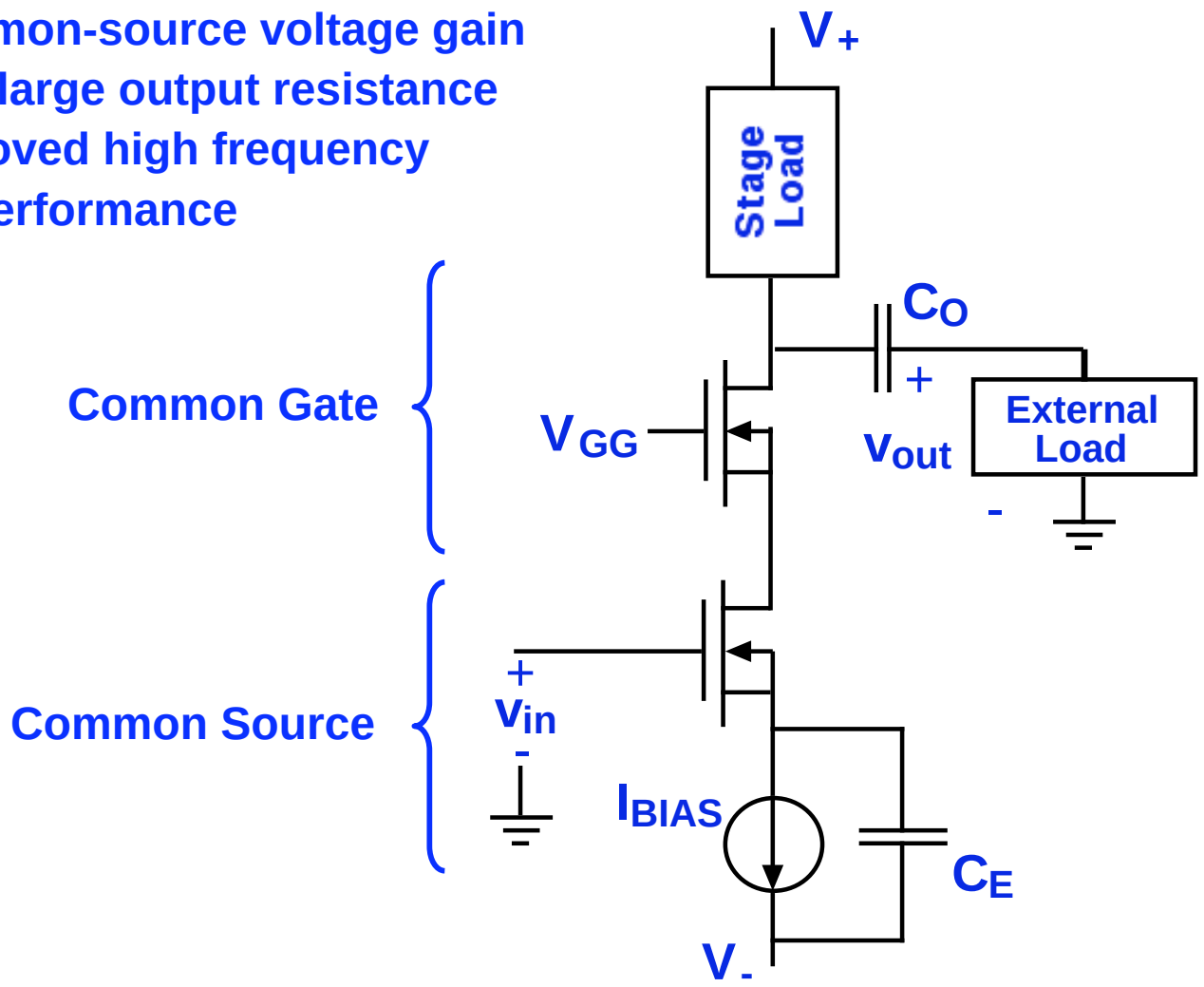


Discussed in Lecture 19.

Specialty Pairings: **The Cascode** (postponed until Lec. 22)

Common-source stage followed by a common gate stage

Common-source voltage gain
Very large output resistance
Improved high frequency performance

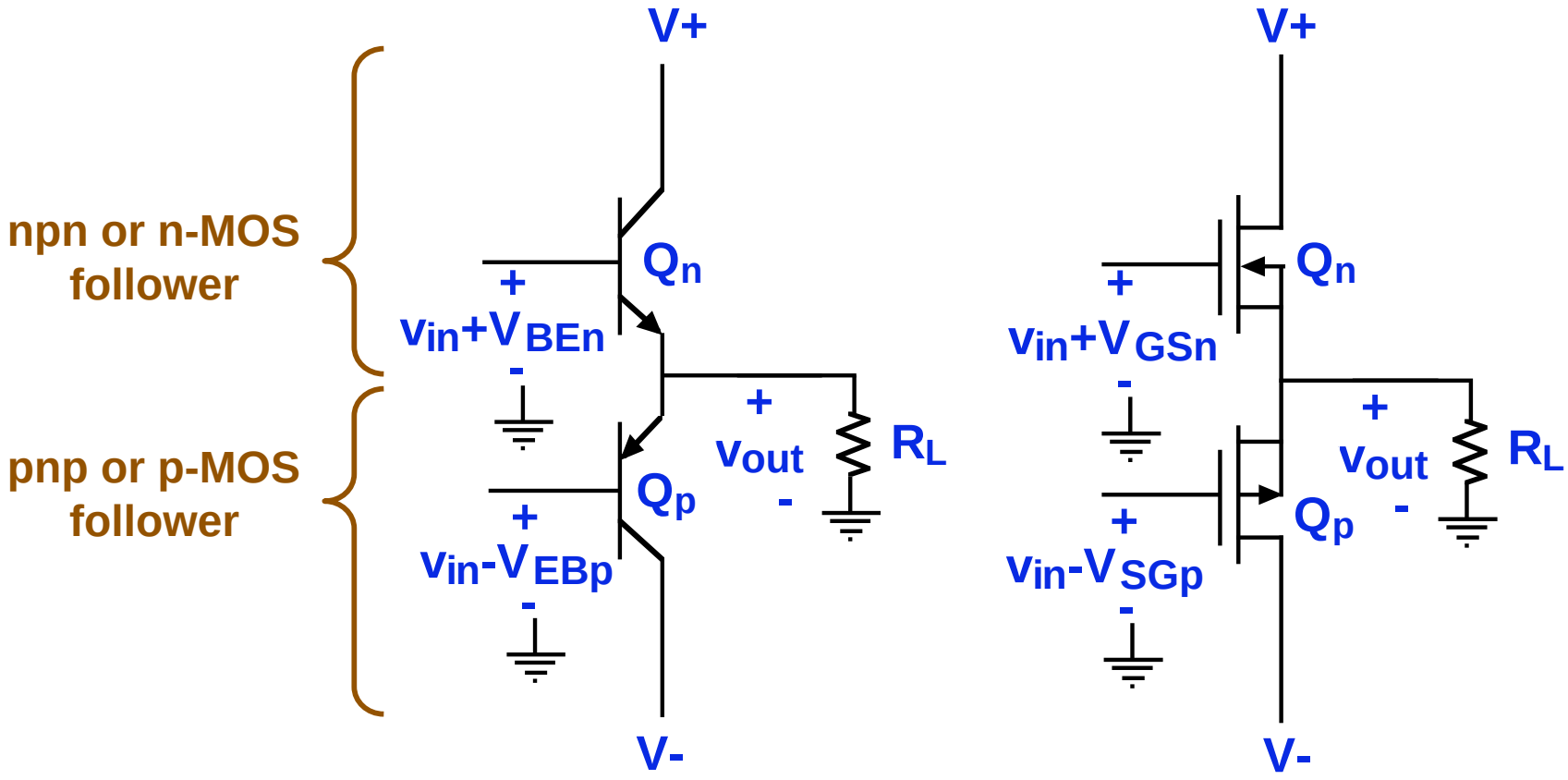


Specialty Pairings: The Push-pull or Totem Pole Output

A stacked pair of complementary emitter- or source-followers

Large input resistance
Small output resistance

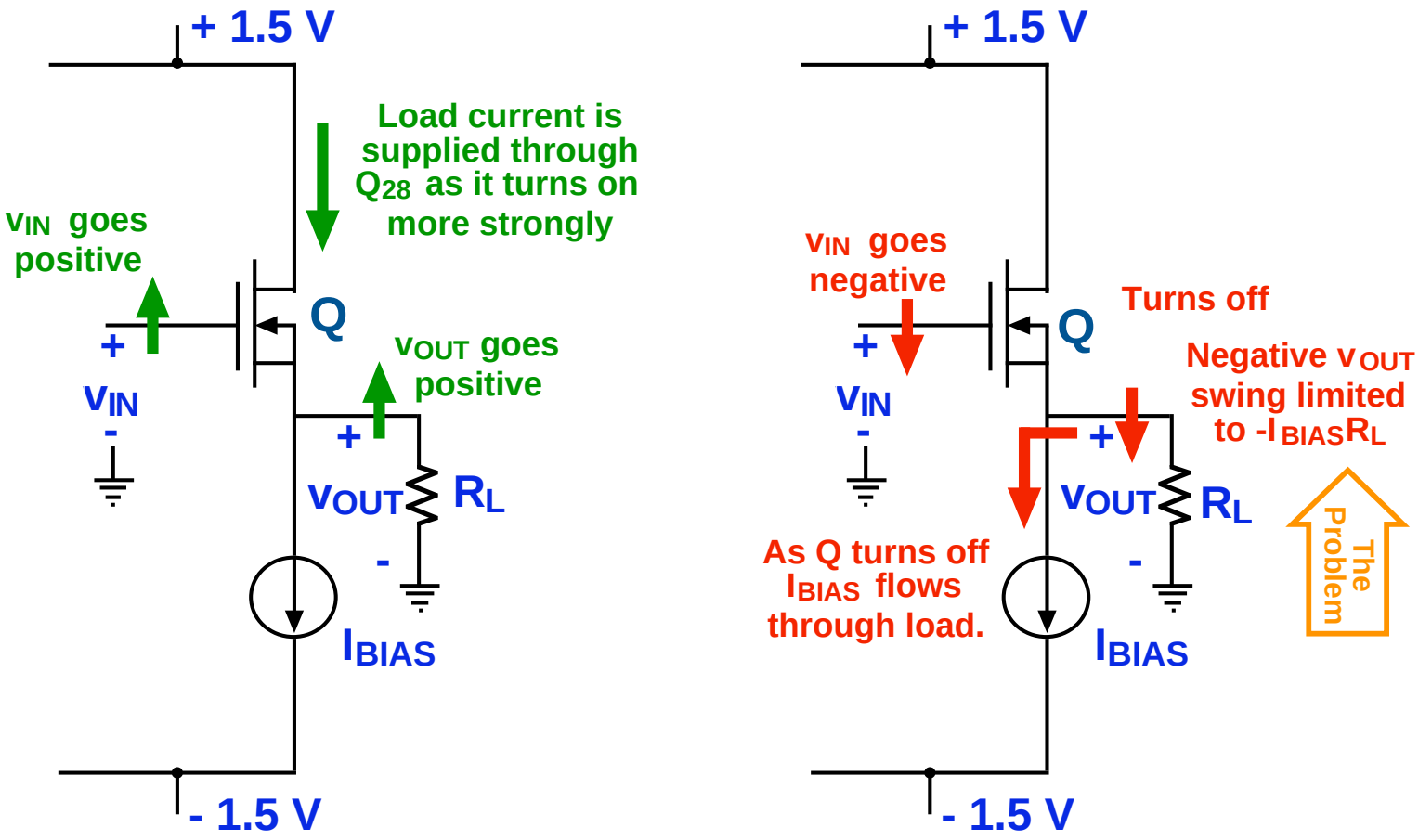
Voltage gain near one
Low quiescent power



Specialty pairings: Push-pull or Totem Pole Output Pairs

The limitations of using a simple follower stage* output:

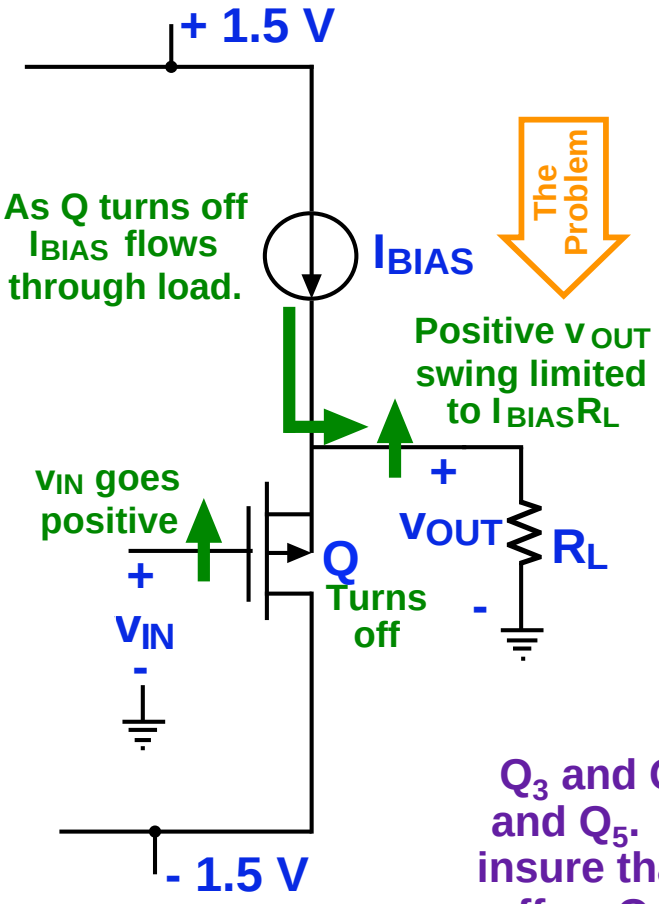
- Using a single source follower as the output stage must be biased with a relatively large drain current to achieve a large output voltage swing, which in turn dissipates a lot of quiescent power.



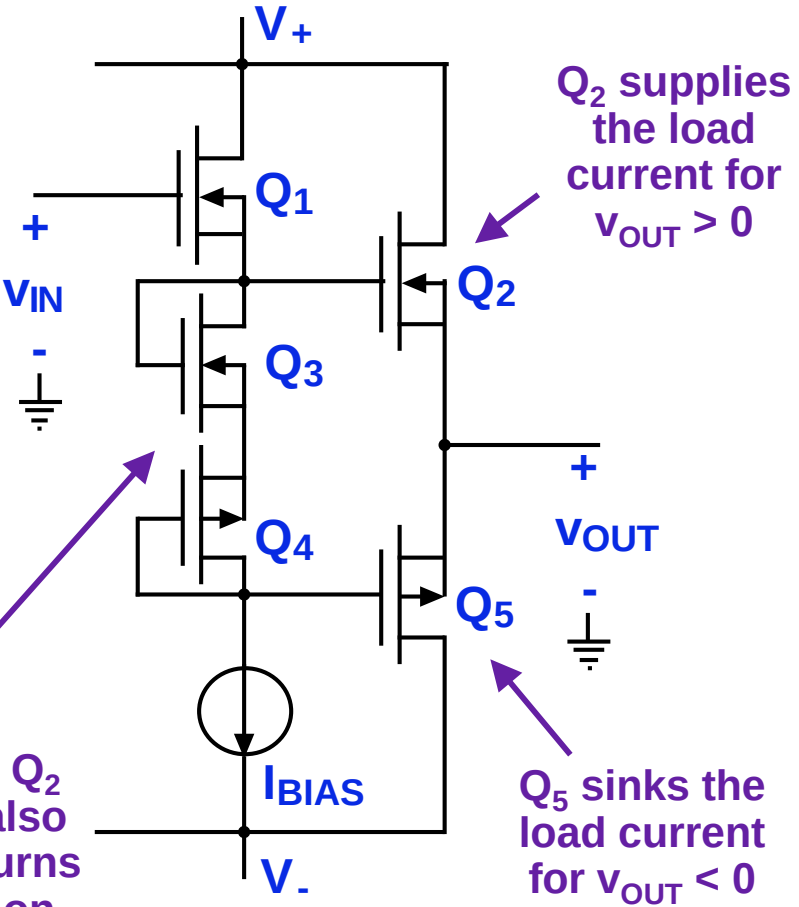
* source follower or emitter follower

Specialty pairings: Push-pull or Totem Pole, cont.

- A p-MOS follower solves the negative swing problem, but has its own positive swing problem.



- The solution is to combine the two in a totem pole stack (and drive and bias them by the preceding stage).

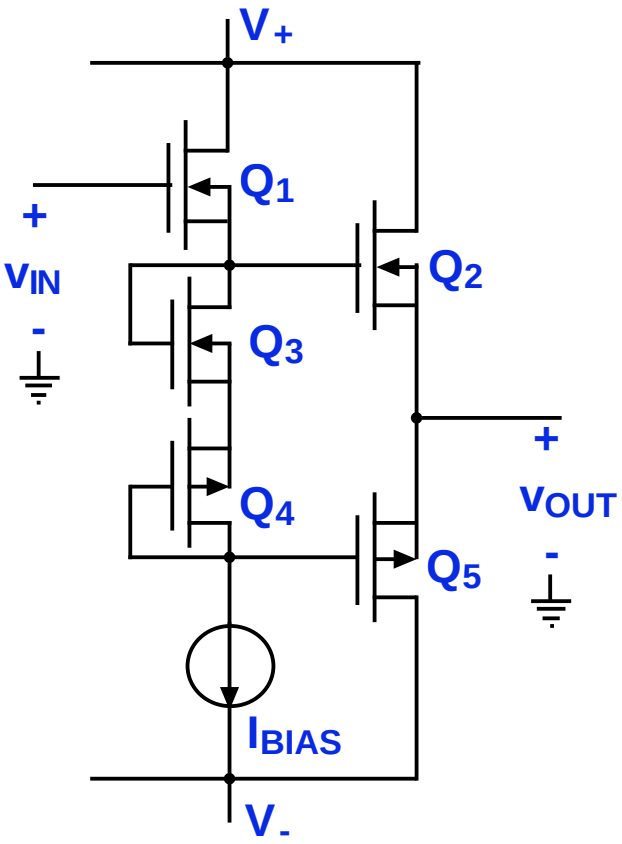


Specialty pairings: Push-pull or Totem Pole, cont.

Comments/Observations:

- The output resistance is largest around $v_{OUT} = 0$. Here both Q_2 and Q_5 are active and the output resistance is:

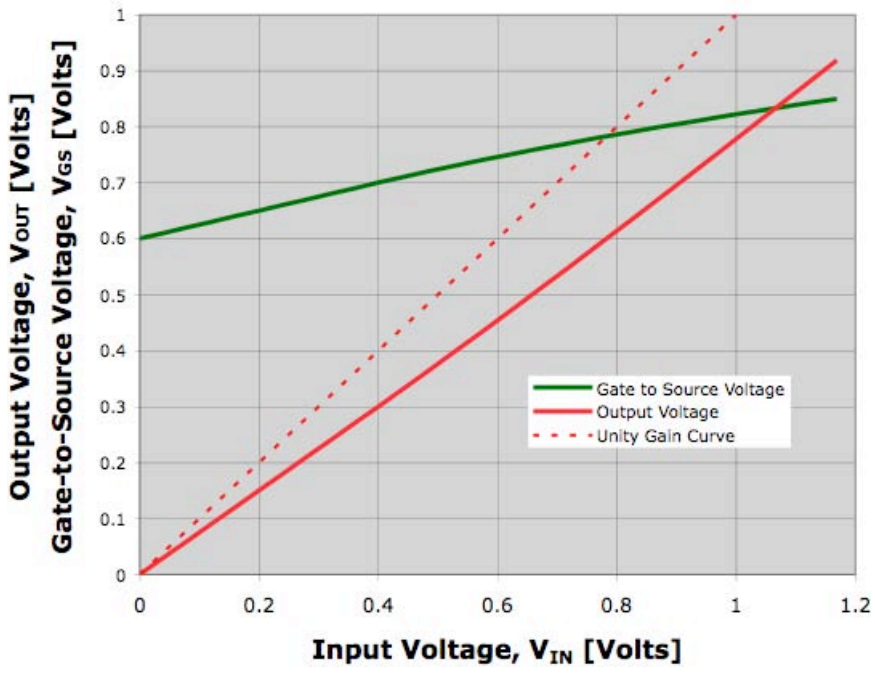
$$r_{out} \approx \frac{1}{g_{m2} + g_{m5}}$$



- One must always make $K_2/K_3 = K_5/K_4$, and in the typical design $K_3 = K_4$, and $K_2 = K_5$. The bias current of Q_2 and Q_5 is set by I_{BIAS}:

$$I_{D2} = |I_{D5}| = (K_2/K_3) I_{BIAS}$$

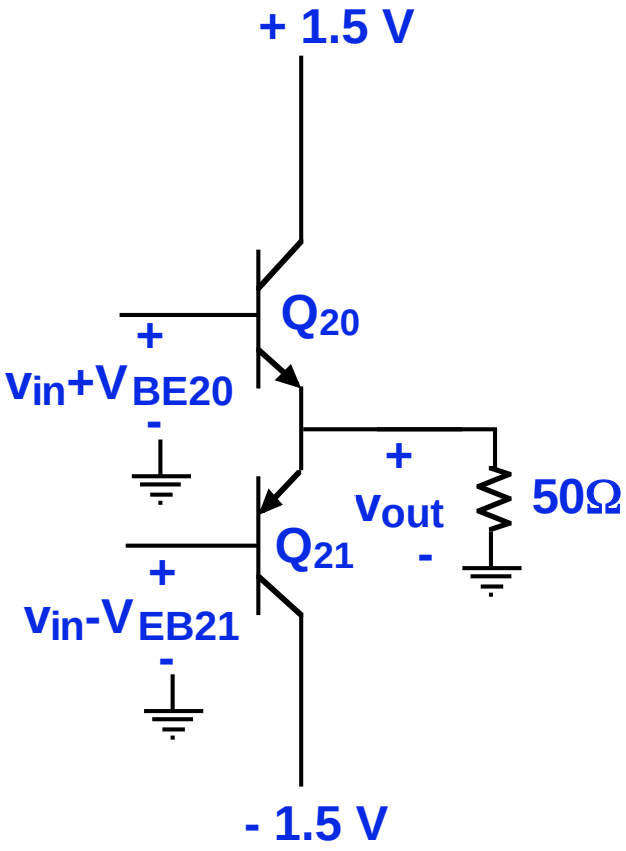
- $|v_{OUT}|$ vs $|v_{IN}|$ is fairly linear over a wide range (see right); $|v_{GS}|$ increases slowly with $|v_{IN}|$.



Specialty pairings: Push-pull or Totem Pole, cont.

Voltage gain:

- The design problem uses a bipolar totem pole. The gain and linearity of this stage depend on the bias level of the totem pole. The gain is higher for with higher bias, but the power dissipation is also.



To calculate the large signal transfer characteristic of the bipolar totem pole we begin with v_{OUT}:

$$v_{OUT} = R_L\left(-i_{E20} - i_{E21}\right)$$

The emitter currents depend on $(v_{IN} - v_{OUT})$:

$$i_{E20} = -I_{E20}e^{(v_{IN}-v_{OUT})/V_t}, \quad i_{E21} = I_{E21}e^{-(v_{IN}-v_{OUT})/V_t}$$

Putting this all together, and using $I_{E21} = -I_{E20}$, we have:

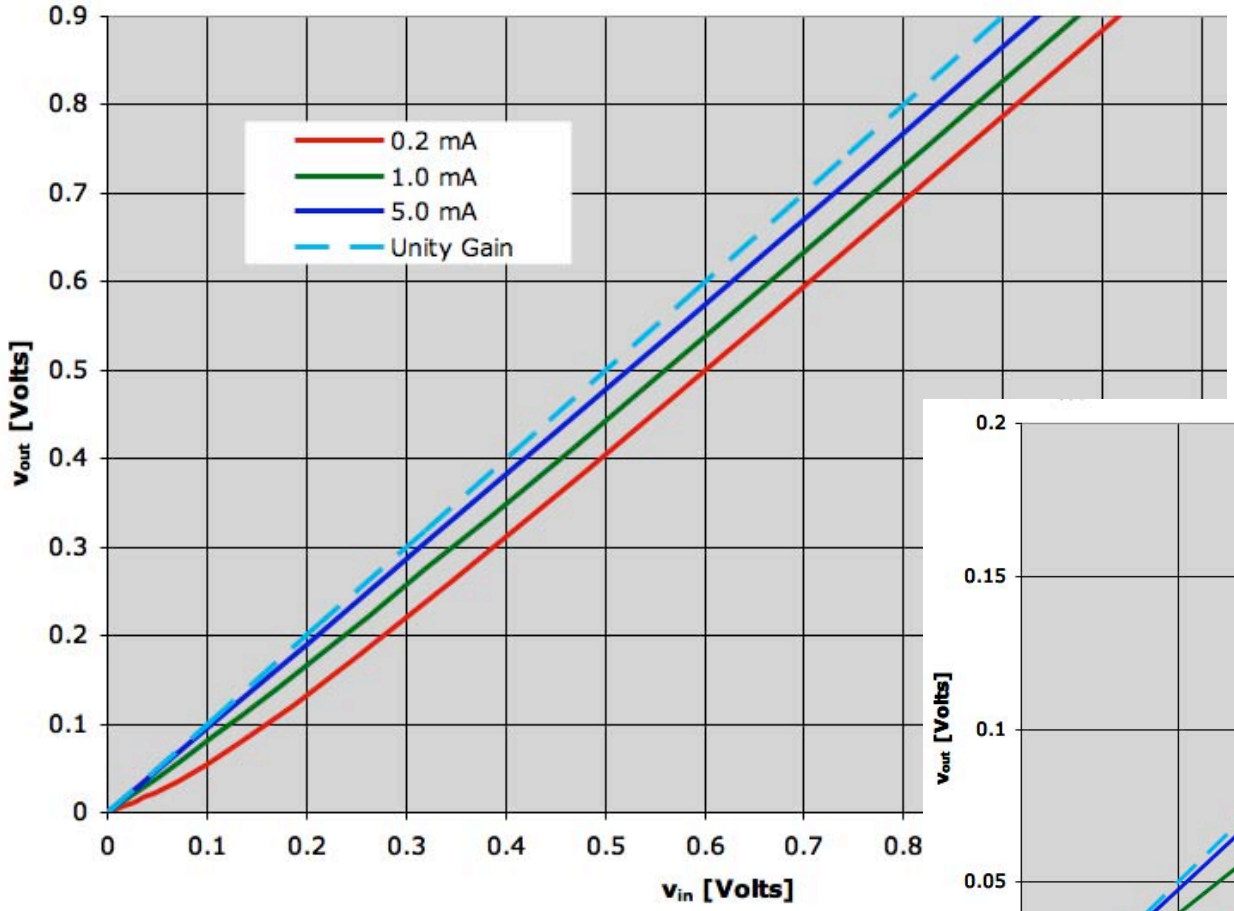
$$v_{out} = R_L I_{E20}\left(e^{(v_{in}-v_{out})/V_t} - e^{-(v_{in}-v_{out})/V_t}\right)$$

$$= 2R_L I_{E20}\sinh\left(v_{in} - v_{out}\right)/V_t$$

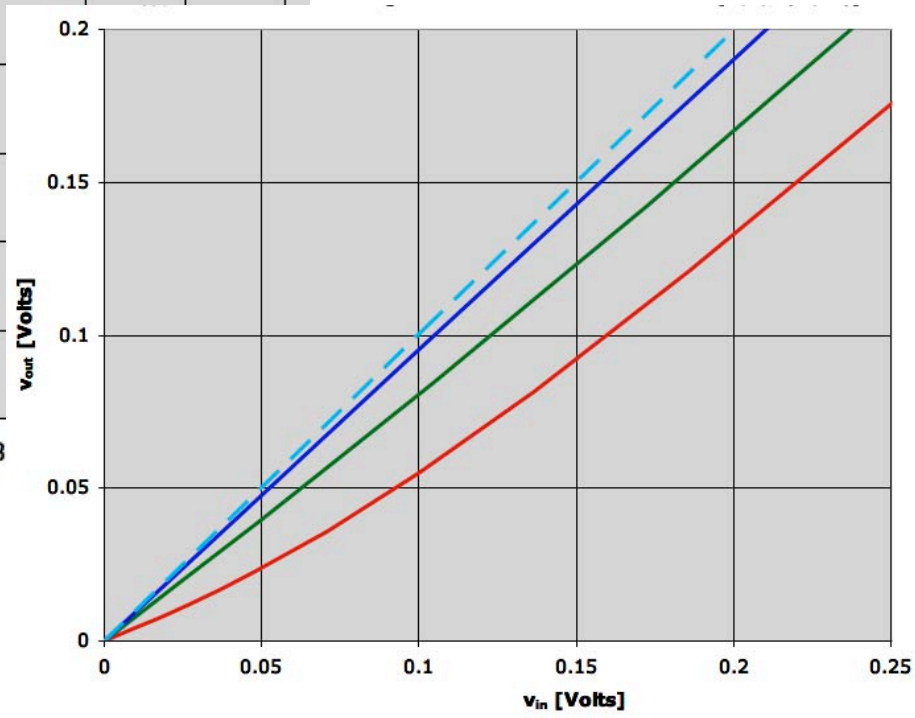
We can do a spread-sheet solution by picking a set of values for $(v_{IN} - v_{OUT})$, using the last equation to calculate the v_{OUT}, using this v_{OUT} to calculate v_{IN}, and finally plotting v_{OUT} vs v_{IN}. The results are seen on the next slide.

Voltage gain, cont.:

- With a 50 Ω load and for several different bias levels we find:



The gain and linearity are improved by increasing the bias current, but the cost is increased power dissipation.



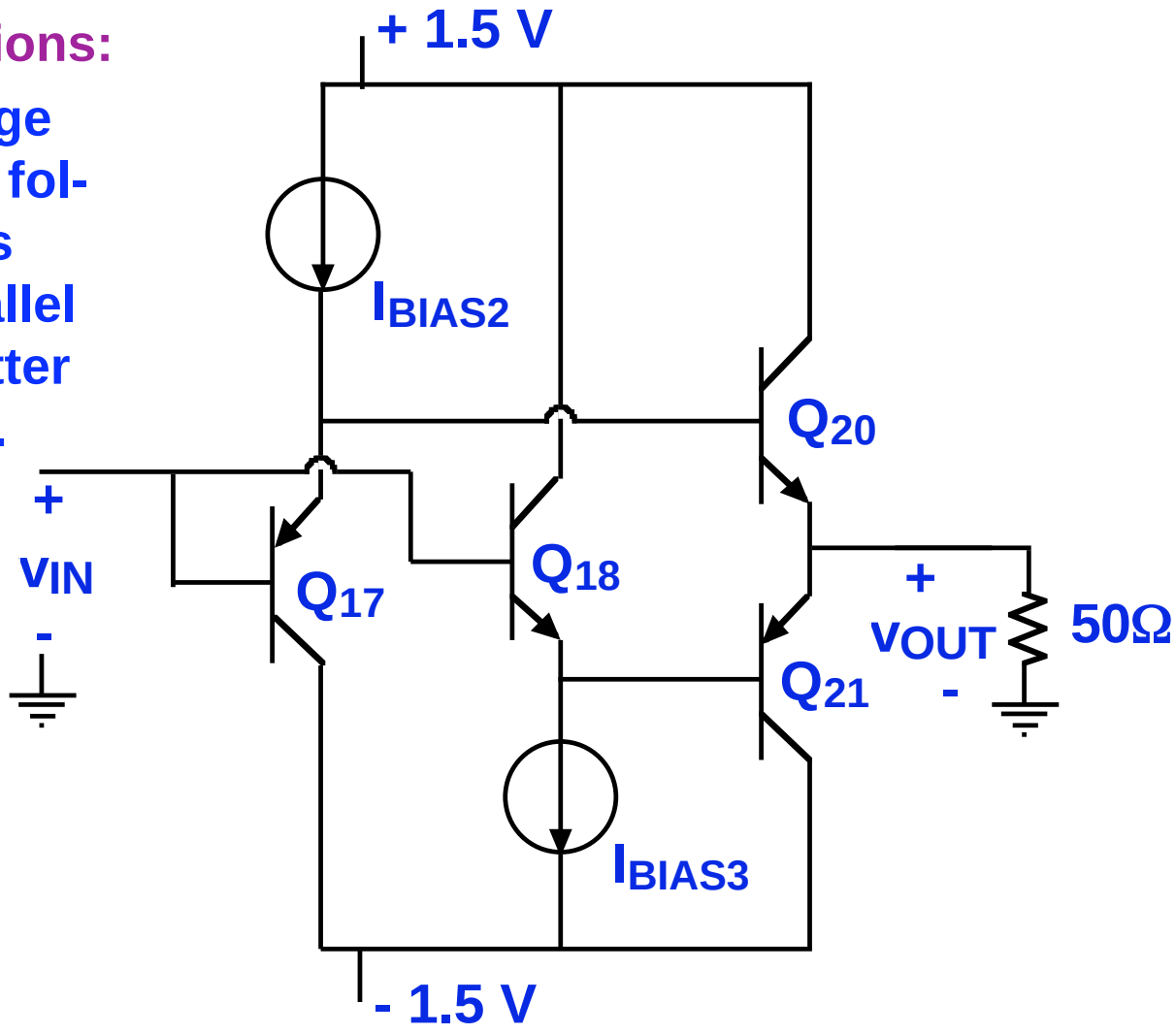
The A_v is lowest and r_{out} is highest at the bias point (i.e., $V_{IN} = V_{OUT} = 0$). r_{in} to the stage is also lowest there.

Specialty pairings: Push-pull or Totem Pole in Design Prob.

Comments/Observations:

- The D.P. output stage involves four emitter follower building blocks arranged as two parallel cascades of two emitter follower stages each.

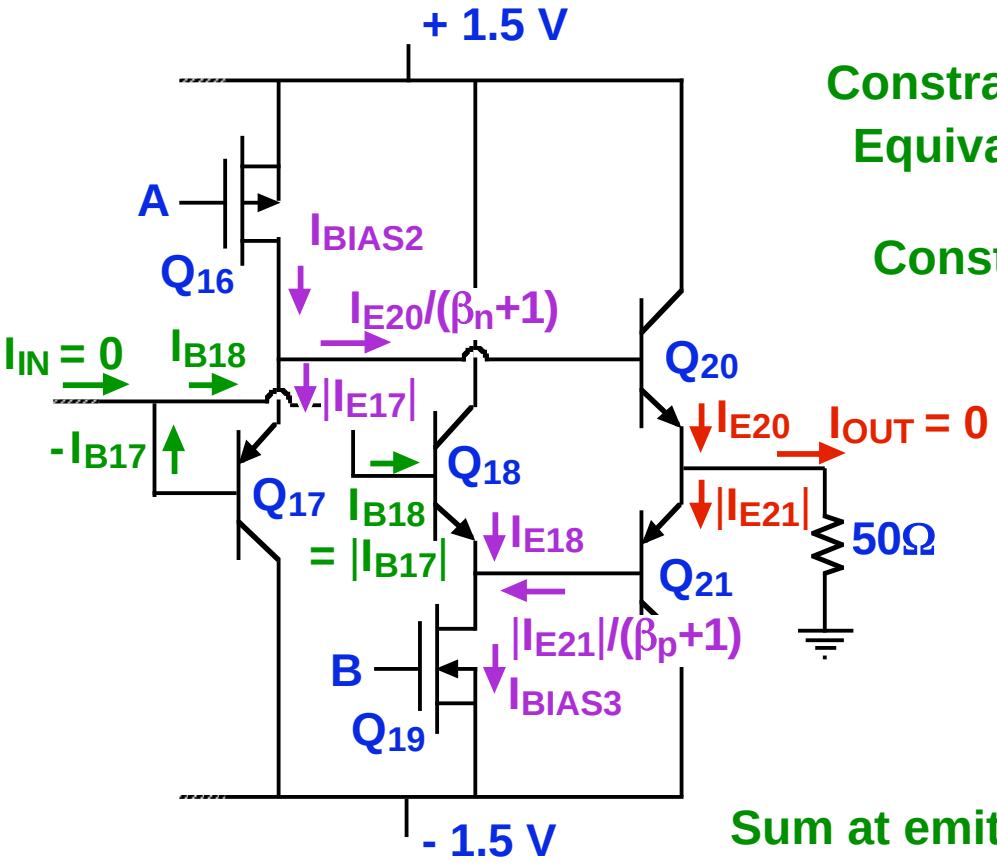
- Driving the totem pole in this manner results in a much larger output voltage range than is obtained by using a single follower as was done in our earlier examples.



NOTE: Designing with this output requires paying special attention to the biasing, and calculating the input and output resistances.

Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Biasing the output stages: getting the currents right



Constraint at input node: $I_{B18} = |I_{B17}|$

Equivalently: $I_{E18}/(\beta_n + 1) = |I_{E17}|/(\beta_p + 1)$

Constraint at output node: $I_{E20} = |I_{E21}|$

Sum at emitter of Q_{20}:

$$I_{BIAS2} = |I_{E17}| + I_{E20}/(\beta_n + 1)$$

$$= (\beta_p + 1)|I_{B17}| + I_{E20}/(\beta_n + 1)$$

$$= (\beta_p + 1)\left[|I_{B17}| + \frac{I_{E20}}{(\beta_n + 1)(\beta_p + 1)}\right]$$

Sum at emitter of Q_{21}:

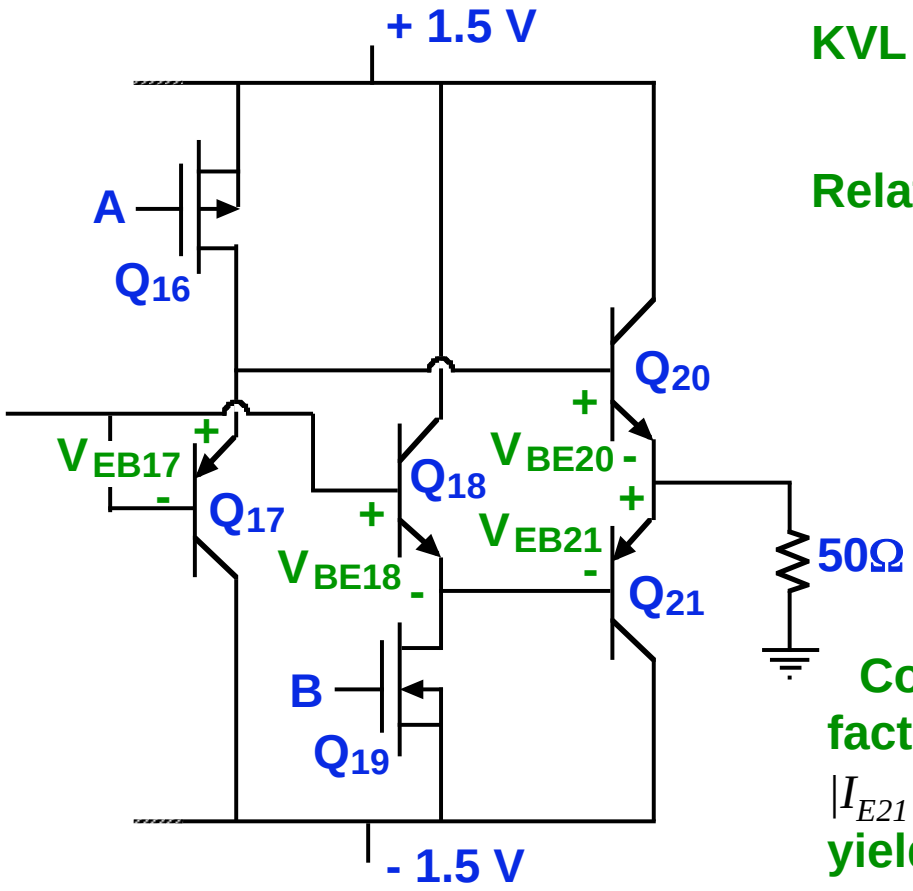
$$I_{BIAS3} = (\beta_n + 1)I_{B18} + |I_{E21}|/(\beta_p + 1) = (\beta_n + 1)\left[I_{B18} + \frac{|I_{E21}|}{(\beta_n + 1)(\beta_p + 1)}\right]$$

Combining everything: $I_{BIAS2}/I_{BIAS3} = (\beta_p + 1)/(\beta_n + 1) \approx \beta_p/\beta_n$

Lesson: The bias currents are constrained.

Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Biasing the output stages: getting the voltages right



KVL constraint:

$$V_{BE20} + V_{EB21} - V_{BE18} - V_{EB17} = 0$$

Relating voltages to currents:

$$V_{EB17} = (kT/q)\ln\left[|I_{E17}|/\gamma_{17} I_{ESp}\right]$$

$$V_{BE18} = (kT/q)\ln\left[I_{E18}/\gamma_{18} I_{ESn}\right]$$

$$V_{BE20} = (kT/q)\ln\left[I_{E20}/\gamma_{20} I_{ESn}\right]$$

$$V_{BE21} = (kT/q)\ln\left[|I_{E21}|/\gamma_{21} I_{ESp}\right]$$

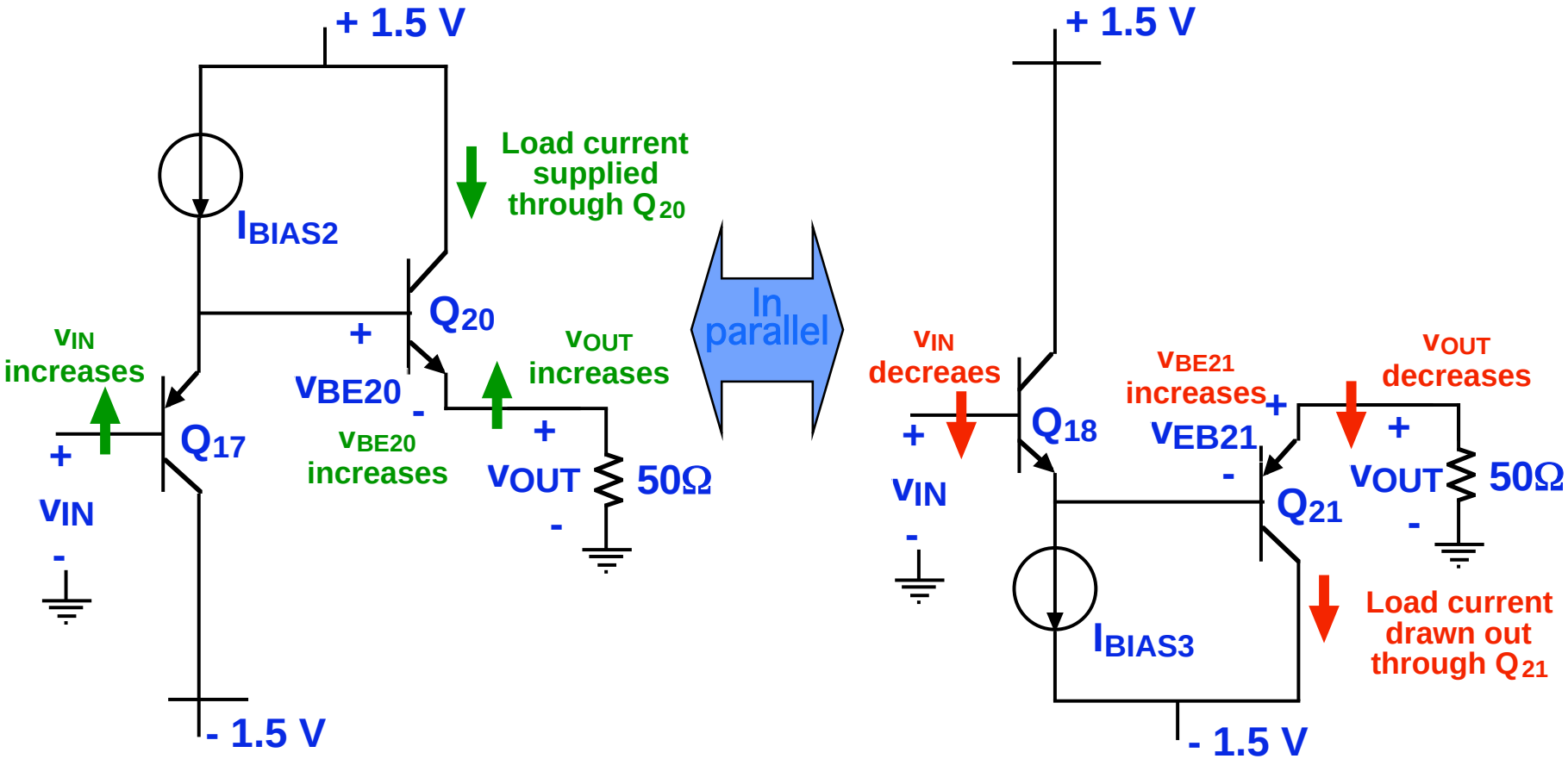
Combining everything, including the fact that $I_{ESp}=I_{ESn}=I_{ES}$, and the results $|I_{E21}|=I_{E20}$ and $|I_{E17}|/(\beta_p+1)=I_{E18}/(\beta_n+1)$, yields:

$$\frac{I_{E20}}{I_{E18}} = \sqrt{\frac{(\beta_p+1)}{(\beta_n+1)}\frac{\gamma_{20}\gamma_{21}}{\gamma_{17}\gamma_{18}}}$$

Lesson: The BJT areas must be properly designed.

Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Operation: The npn follower supplies current when the input goes positive to push the output up, while the pnp follower sinks current when the input goes negative to pull the output down.

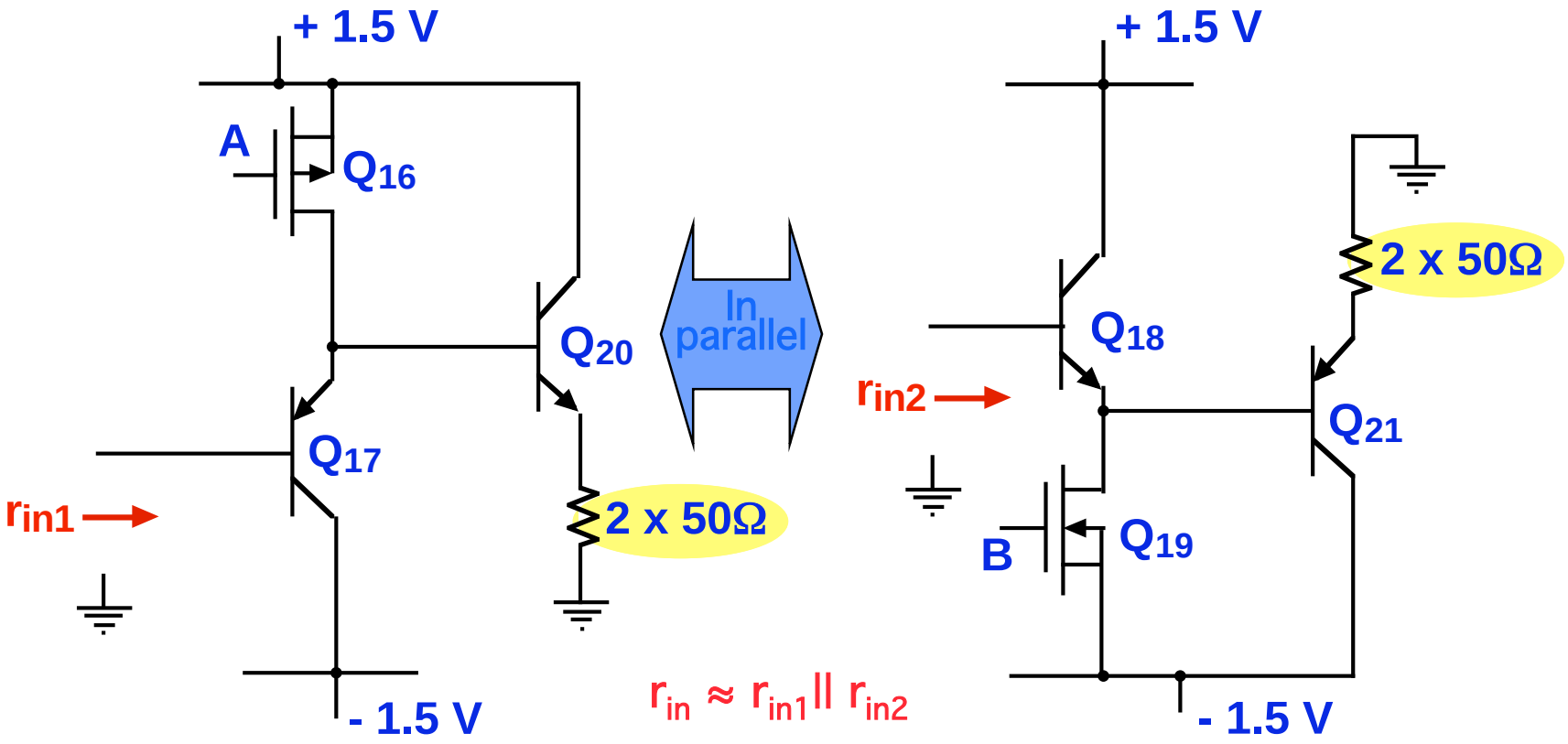


NOTE: Near $v_{in} = 0$ we have two paths in parallel, and this must be considered when finding r_{in} and r_{out}.

Specialty pairings: Push-pull or Totem Pole in D.P., cont.

The input resistance of the output stages as seen by the Current Mirror

We will make the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the input resistance.

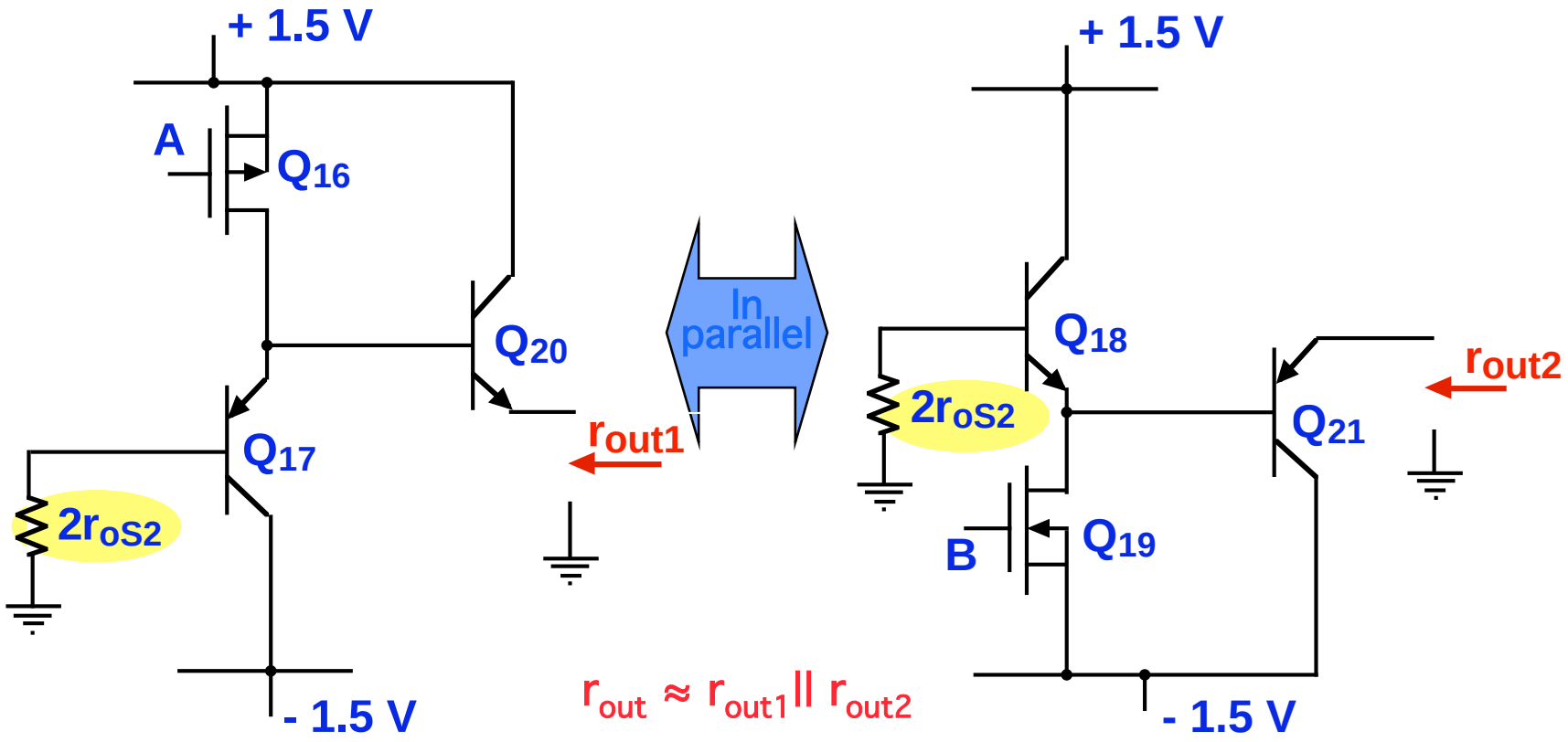


Note: r_{in} is smallest around $v_{in} = 0$, so this is a worst-case estimate.

Specialty pairings: Push-pull or Totem Pole in D.P., cont.

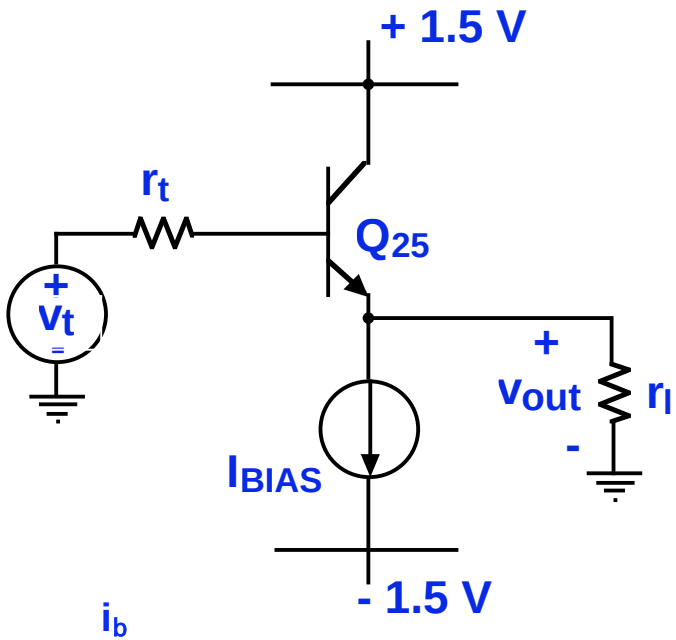
The output resistance of the amplifier as seen by the 50 Ω load

We will make the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the output resistance.

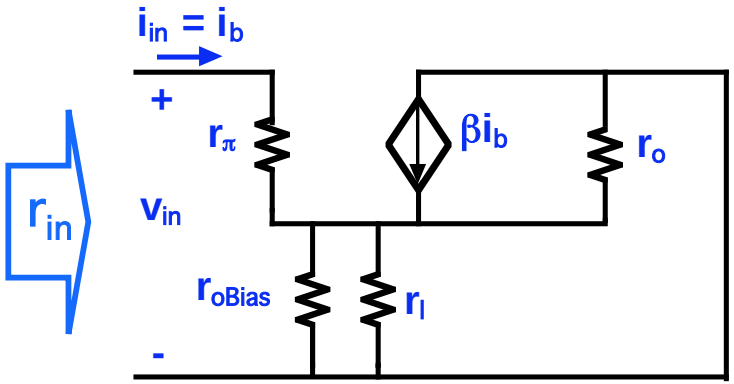


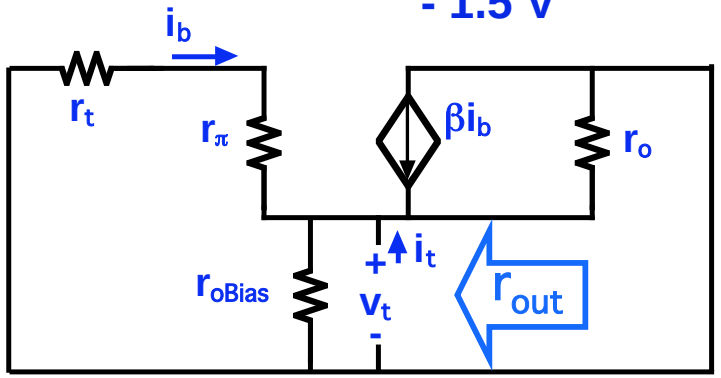
Note: r_{out} is largest around $v_{out} = 0$, so this is a worst-case estimate.

Specialty pairings: Push-pull or Totem Pole in D.P., cont.



Reviewing the input and output resistances of an emitter follower:





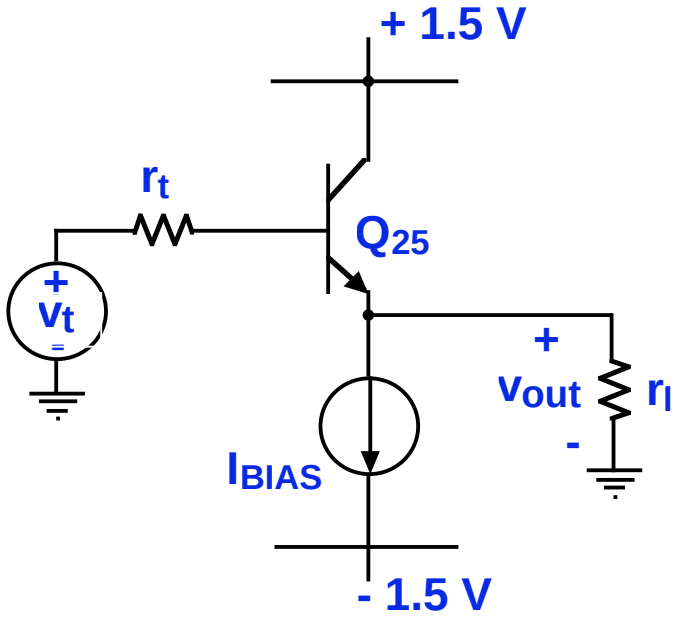
$$r_{in} = r_\pi + (\beta+1)(r_l \parallel r_o \parallel r_{Bias}) \approx r_\pi + (\beta+1)r_l$$

$$r_{out} = 1/\left[g_o + g_{Bias} + (\beta+1)/(r_\pi + r_t)\right] \approx (r_\pi + r_t)/(\beta+1)$$

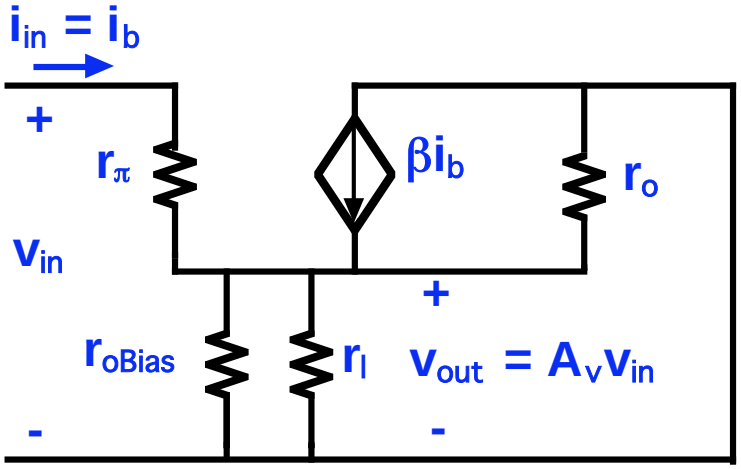
Note:

- **Looking in the resistance is multiplied by (β+1); looking back it is divided by (β+1).**

Specialty pairings: Push-pull or Totem Pole in D.P., cont.



Reviewing the voltage gain of an emitter follower:



$$v_{out} = (\beta+1) i_b (r_l \,||\, r_o \,||\, r_{Bias})$$

$$v_{in} = i_b r_\pi + (\beta+1) i_b (r_l \,||\, r_o \,||\, r_{Bias})$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{(\beta+1)(r_l \,||\, r_o \,||\, r_{Bias})}{r_\pi + (\beta+1)(r_l \,||\, r_o \,||\, r_{Bias})}$$

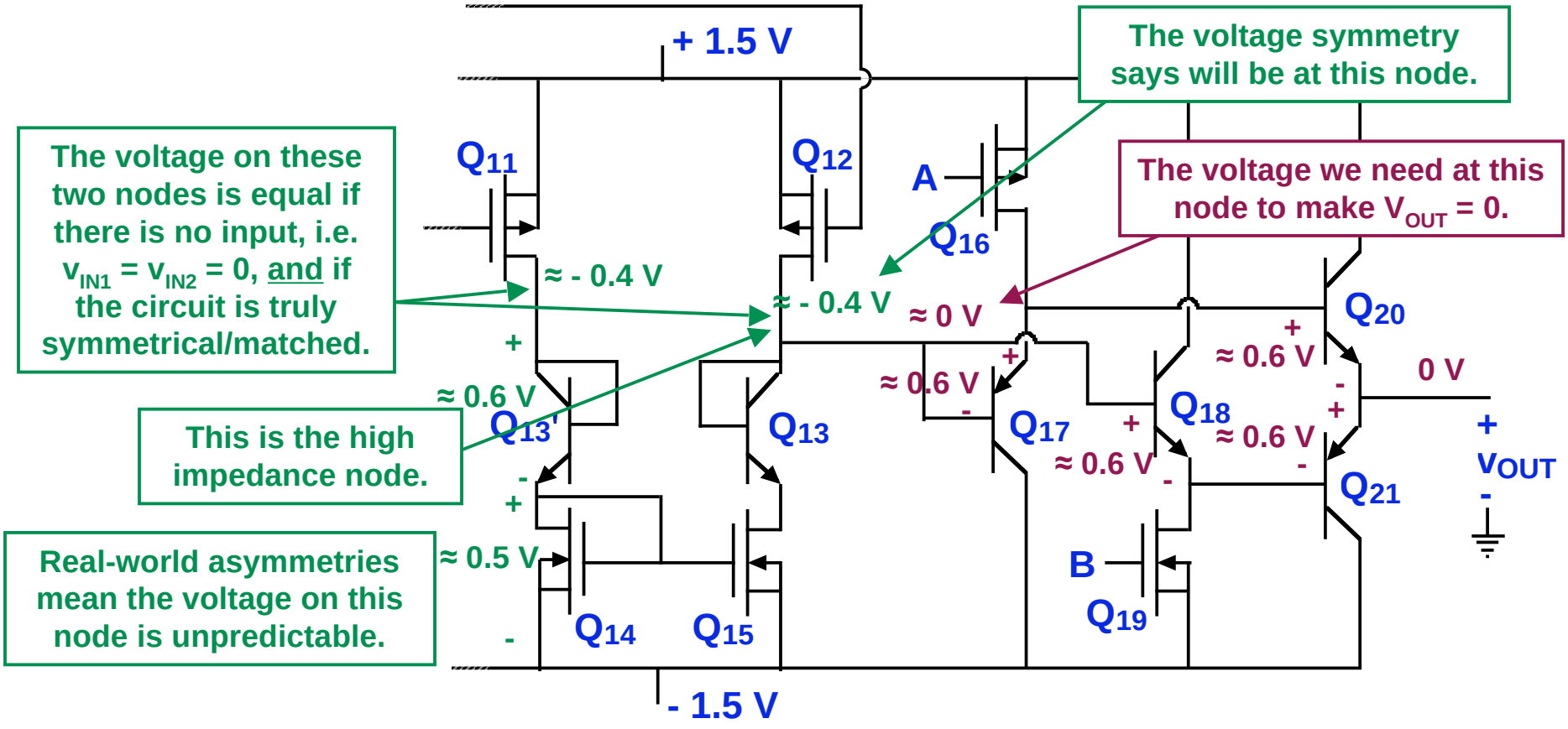
$$\approx \frac{(\beta+1) r_l}{r_\pi + (\beta+1) r_l}$$

Note: The voltage gains of the third-stage emitter followers (Q_{17} and Q_{18}) will likely be very close to one, but that of the stage-four followers might be noticeably less than one.

DC off-set at the output of an Operational Amplifier:

DC off-set:

The node between Q_{12} and Q_{13} is a high impedance node whose quiescent voltage can only be determined by invoking symmetry.*



In any practical Op Amp, a very small differential input, v_{IN1}-v_{IN2}, is require to make the voltage on this node (and V_{OUT}) zero.

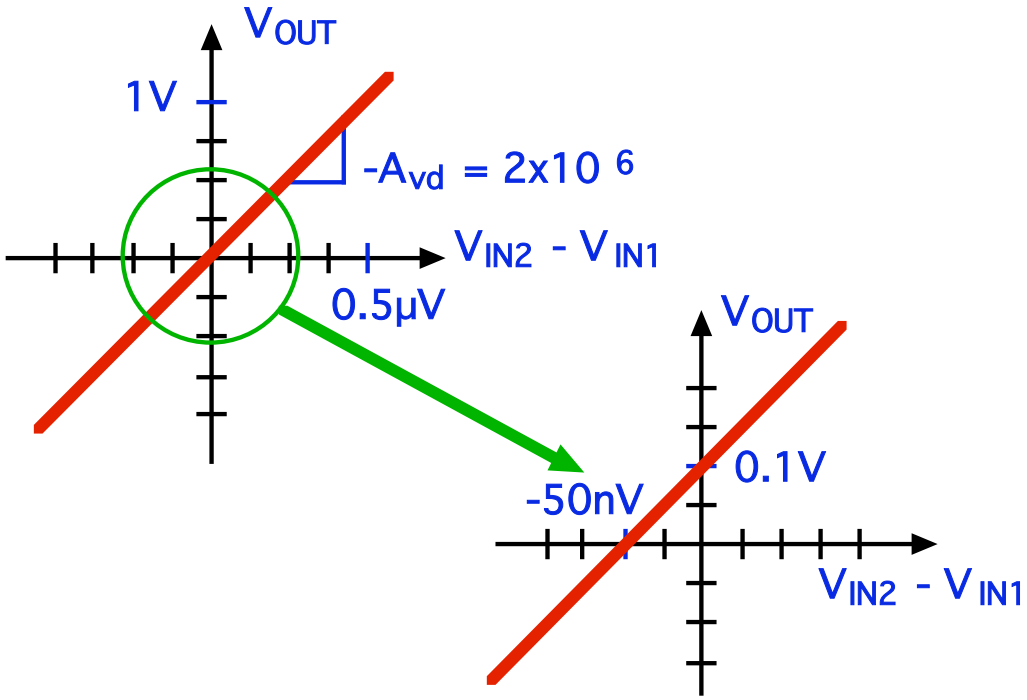
DC off-set at the output of an Op Amp, cont:

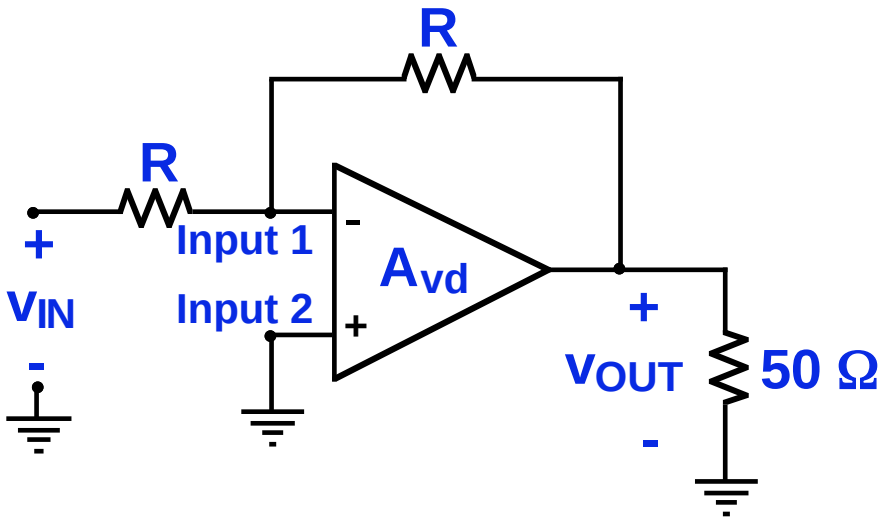
DC off-set:

The transfer characteristic, v_{OUT} vs $(v_{IN1} - v_{IN2})$, will not in general go through the origin, i.e.,

$$v_{OUT} = A_{vd}(v_{IN1} - v_{IN2}) + V_{OFFSET}$$

In the example in the figure A_{vd} is -2 x 10^6, and V_{OFFSET} is 0.1 V.



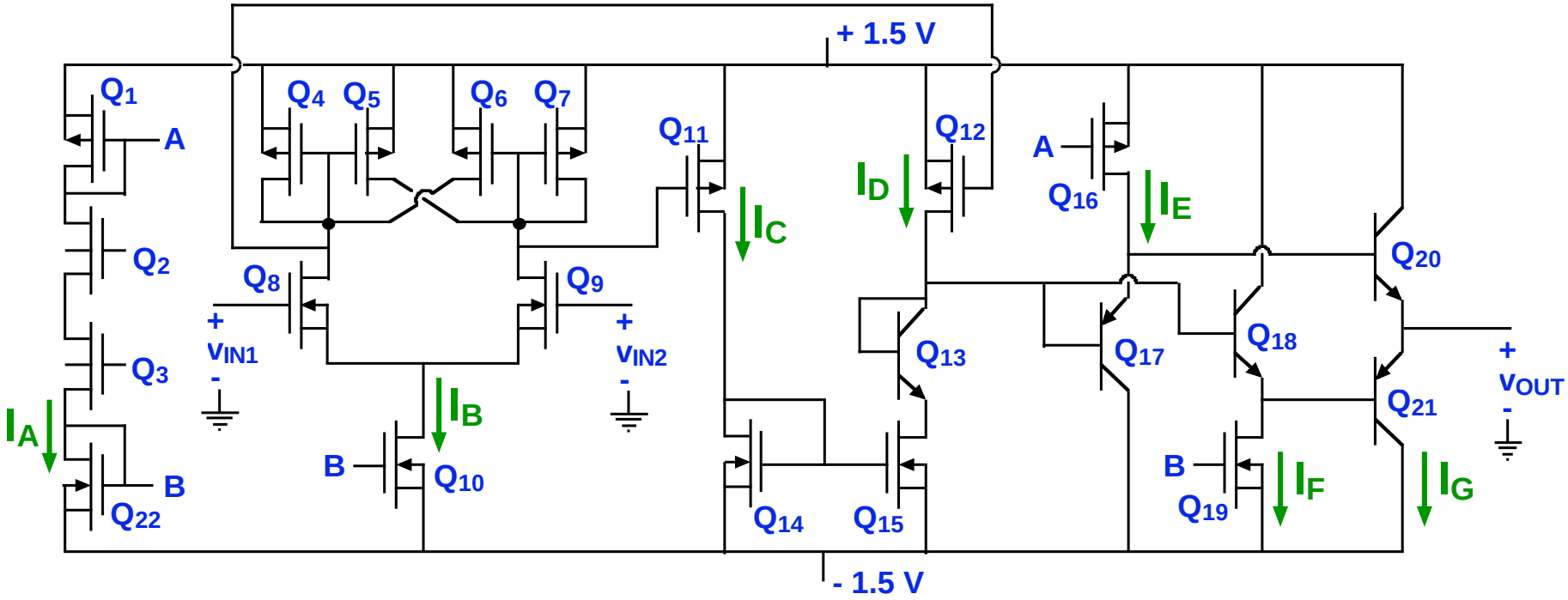


In a practice, an Op Amp will be used in a feed-back circuit like the example shown to the left, and the value of v_{OUT} with v_{IN} = 0 will be quite small. For this example (in which A_{vd} = -2 x 10^6, and V_{OFFSET} = 0.1 V) v_{OUT} is only 0.1 µV.

In the D.P. you are asked for this value for your design.

Power dissipation calculation

A constraint on the bias currents is the total power dissipation specification of 8.5 mW. This means that the total bias current must be ≈ 2.8 mA or less (i.e, 3 V x 2.8 mA ≈ 8.5 mW).



$$P_Q = \left(I_A + I_B + I_C + I_D + I_E + I_F + I_G\right) \times 3\,Volts$$

$$I_A + I_B + I_C + I_D + I_E + I_F + I_G \leq 2.8\,mA$$

Lecture 21 - Diff-Amp Analysis II - Summary

- **Active loads - Lee load, Current mirror**
  - **New CM analysis foils**
- **Specialty stages - useful pairings**
  - **Source coupled pairs:** MOS
  - **Cascode:** Postponed until Lecture 22
  - **Push-pull output:** Emitter followers in vertical chain
    - Very low output resistance
    - Shared duties for positive and negative output swings
- **Diff Amp Metrics**
  - **Output resistance:** Largest about zero; view as followers in parallel
  - **DC off-set on output:** Nulled out by slight differential mode input
  - **Power consumption:** Add up the current from the supplies

Happy Thanksgiving

6.012 Microelectronic Devices and Circuits

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