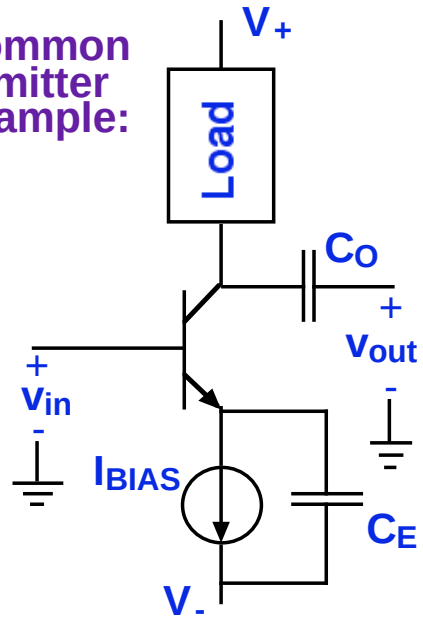
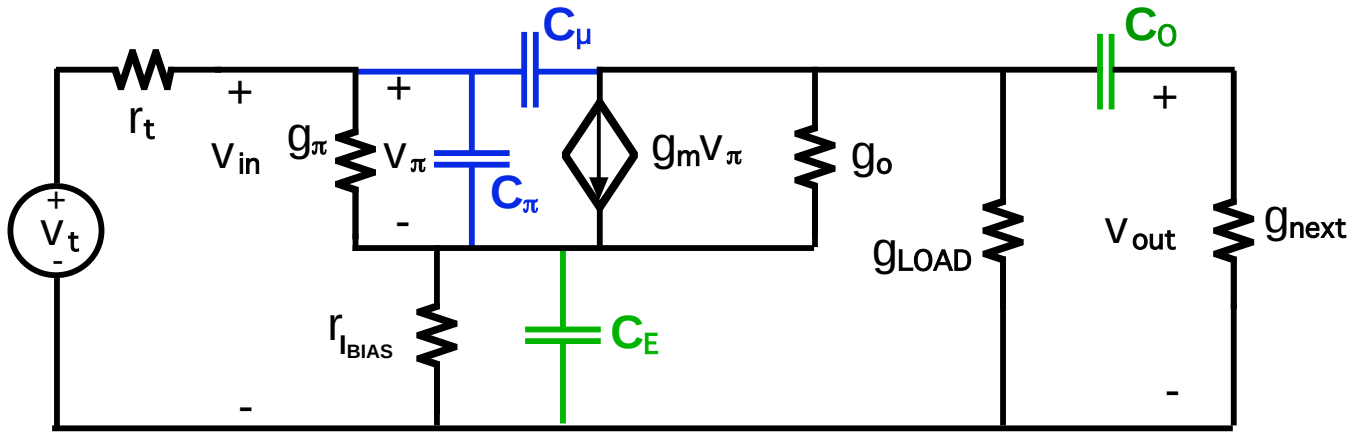
Lecture 18 - Single Transistor Amplifier Stages - Outline

- **Announcements**
  - **Exam Two Results -** Exams will be returned tomorrow (Nov 13).
- **Review - Biasing and amplifier metrics**
  - **Mid-band analysis:** Biasing capacitors: short circuits above ω_{LO}
    Device capacitors: open circuits below ω_{HI}
    Midband: $\omega_{LO} < \omega < \omega_{HI}$
  - **Current mirror current source/sink biasing:** on source terminal
  - **Performance metrics:** gains (voltage, current, power); input and output resistances; power dissipation; bandwidth
  - **Multi-stage amplifiers:** two-port analysis; current source/sink chains
- **Building-block stages**
  - **Common source**
  - **Common gate**
  - **Source follower** (also called "common drain")
  - **Series feedback** (more commonly: "source degeneracy")
  - **Shunt feedback**

Mid-band: the frequency range of constant gain and phase

Common emitter example:

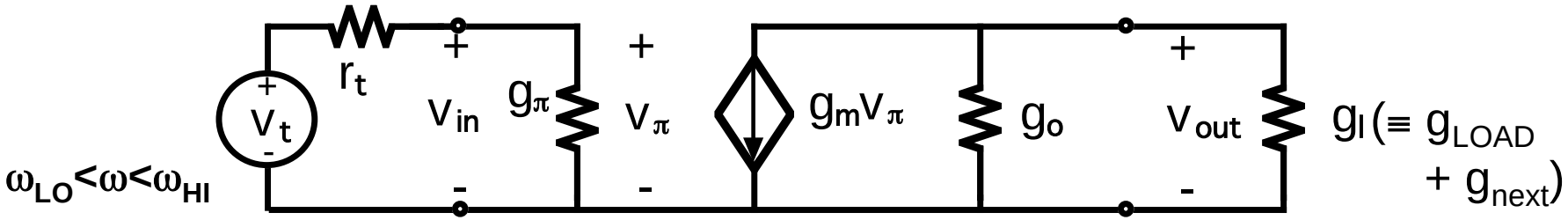




Biasing capacitors: effective shorts $\omega > \omega_{LO}$

Device capacitors: effective open circuits $\omega < \omega_{HI}$

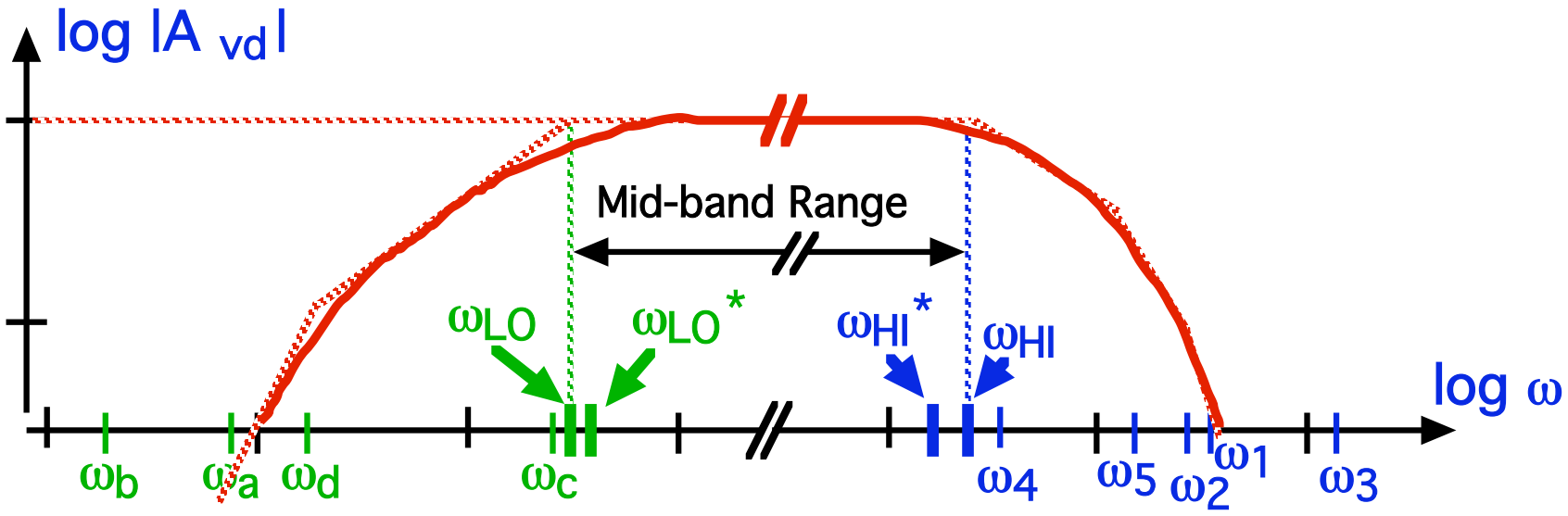
We call the frequency range between ω_{LO} and ω_{HI}, the "mid-band" range. For frequencies in this range our model is simply:



Valid for $\omega_{LO} < \omega < \omega_{HI}$, the "mid-band" range, where all bias capacitors are shorts and all device capacitors are open.

Mid-band, cont: The mid-band range of frequencies

In this range of frequencies the gain is a constant, and the phase shift between the input and output is also constant (either 0° or 180°).



All of the parasitic and intrinsic device capacitances are effectively open circuits

All of the biasing and coupling capacitors are effectively short circuits

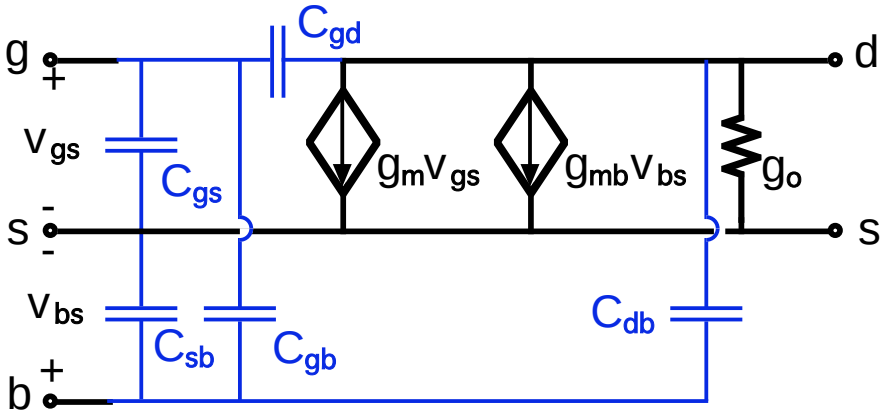
*** We will learn how to estimate ω_{HI} and ω_{LO} in Lectures 23/24.**

Linear equivalent circuits for transistors (dynamic):

Collecting our results for the MOSFET and BJT biased in FAR

No velocity saturation; $\alpha = 1$

MOSFET:



$$g_m = K[V_{GS} - V_T(V_{BS})][1 + \lambda V_{DS}] \approx \sqrt{2KI_D}$$

$$g_o = \frac{K}{2}[V_{GS} - V_T(V_{BS})]^2 \lambda \approx \lambda I_D = \frac{I_D}{V_A}$$

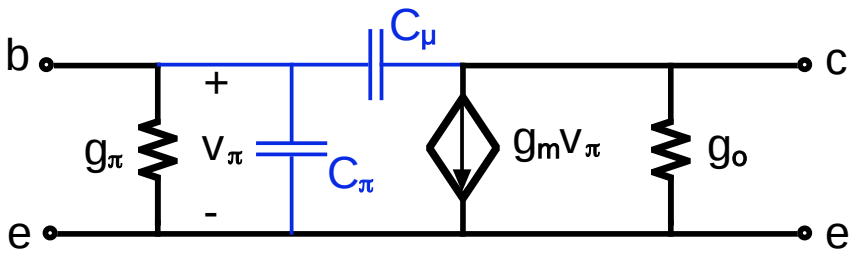
$$g_{mb} = \eta g_m = \eta \sqrt{2KI_D}$$

with $$\eta \equiv -\left.\frac{\partial V_T}{\partial v_{BS}}\right|_Q = \frac{1}{C_{ox}^*}\sqrt{\frac{\varepsilon_{Si} q N_A}{|q\phi_p| - V_{BS}}}$$

$C_{gs} = \frac{2}{3} W L C_{ox}^*$, C_{sb}, C_{gb}, C_{db} : depletion capacitances

$C_{gd} = W C_{gd}^*$, where C_{gd}^* is the G-D fringing and overlap capacitance per unit gate length (parasitic)

BJT:



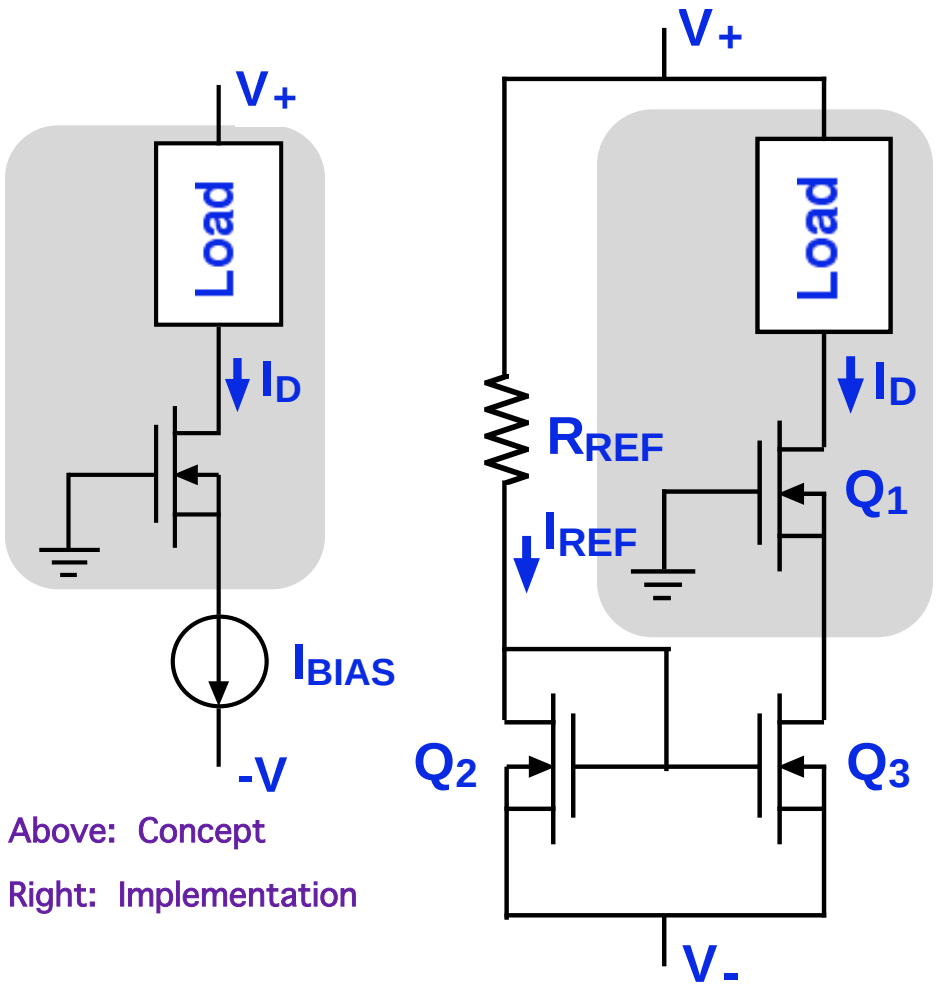
$$g_m = \frac{q}{kT}\beta_o I_{BS} e^{qV_{BE}/kT}[1 + \lambda V_{CE}] \approx \frac{qI_C}{kT}$$

$$g_\pi = \frac{g_m}{\beta_o} = \frac{qI_C}{\beta_o kT}$$

$$g_o = \beta_o I_{BS}\left[e^{qV_{BE}/kT} + 1\right]\lambda \approx \lambda I_C = \frac{I_C}{V_A}$$

$C_\pi = g_m \tau_b +$ B-E depletion cap. with $\tau_b \equiv \frac{w_B^2}{2D_e}$, C_μ : B-C depletion cap.

Biasing a MOSFET stage with a MOSFET current mirror:



Above: Concept

Right: Implementation

Note: Q_2 is always in saturation. As long as Q_3 is also in saturation, its drain current will be $(K_{Q3}/K_{Q2})\ I_{REF}$.

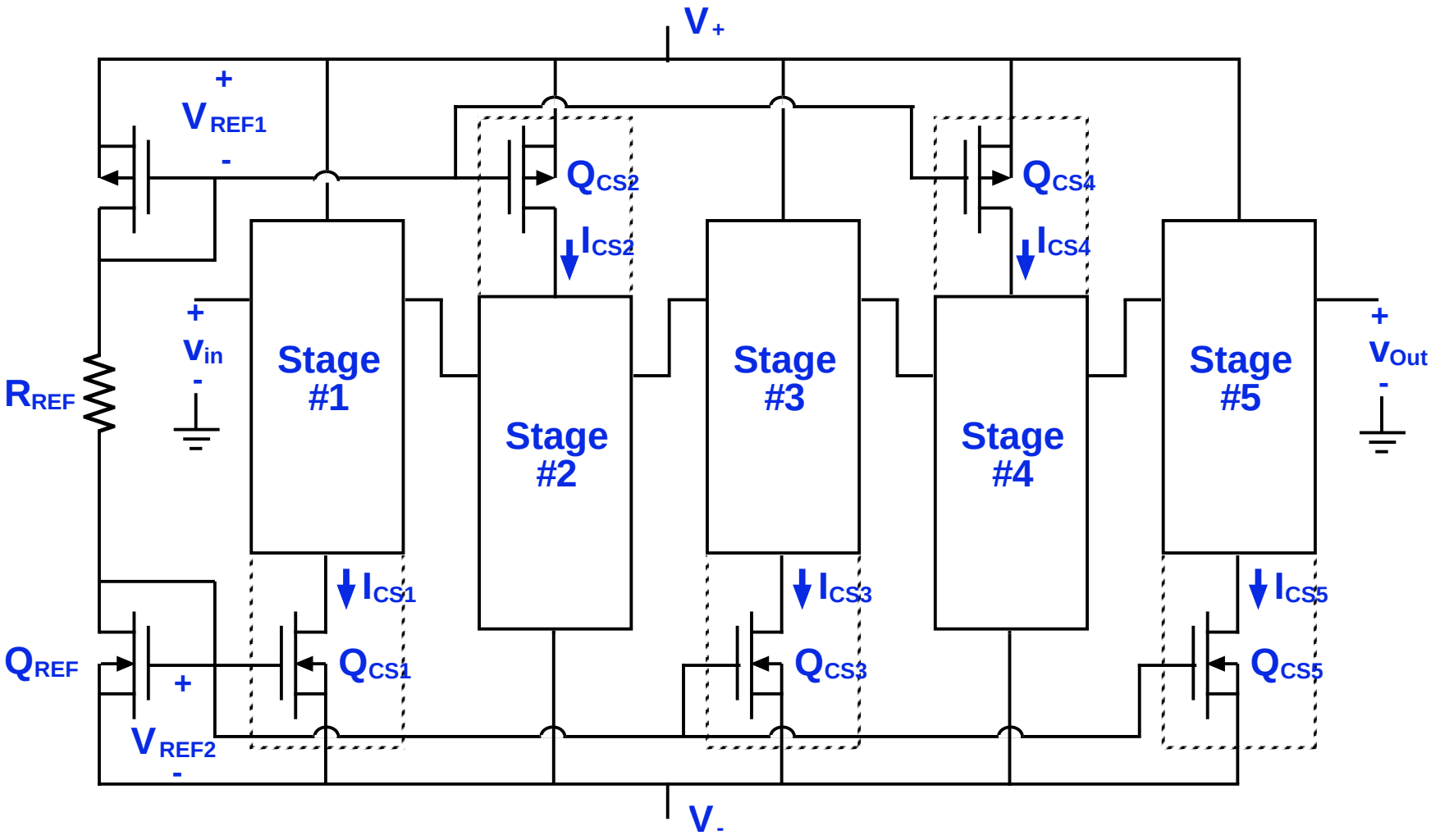
The design process:

- We have a target I_D, and we want to know what size to make R_{REF} to get it.
- For simplicity we can make $K_{Q3} = K_{Q2}$, so $I_{REF} = I_D$.
- Select a K_{Q2}, perhaps that corresponding to a mini-mum size device.
- Calculate what V_{GS2} (= V_{REF}) is when Q_2's drain current is I_{REF}: $V_{REF} = V_T - (2\ I_{REF}/K_{Q2})^{1/2}$
- What R_{REF} must be to make Q_2's drain current I_{REF} can then be found from:

$$R_{REF} = [(V_+ - V_-) - V_{REF}]/I_{REF}$$

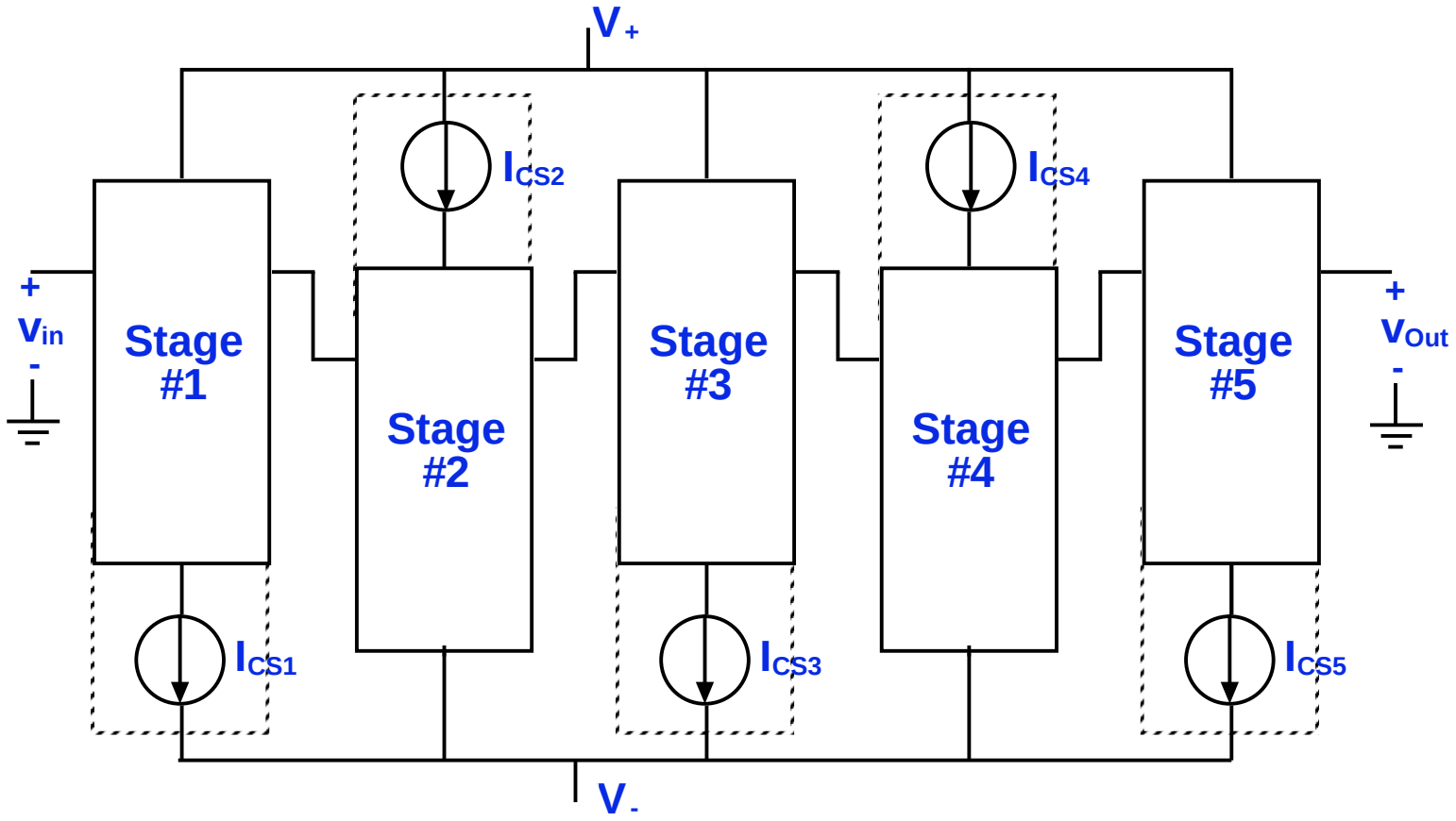
- If R_{REF} has this value, then Q_3's drain current will be I_{REF} as long as it is in saturation.

Linear amplifier basics: Biasing multi-stage amplifiers



⇒ The current mirror voltage reference method can be extended to bias multiple stages, and one reference chain can be used to provide V_{REF} to all the sources and sinks in an amplifier.

Linear amplifier basics: Biasing multi-stage amplifiers. cont.

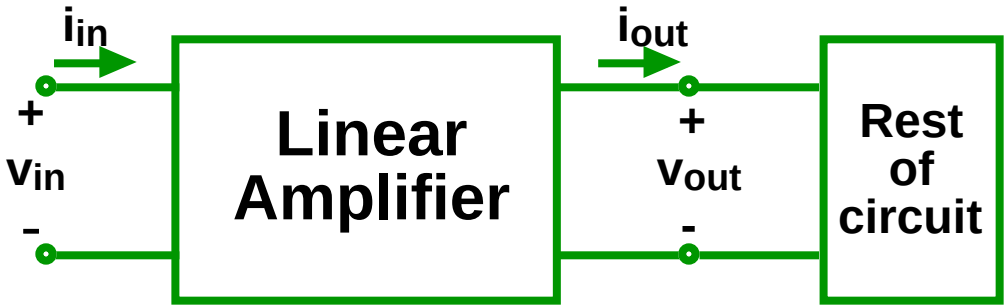


When looking at a complex circuit schematic it is useful to identify the voltage reference chain and the biasing transistors and replace them all by current source symbols.

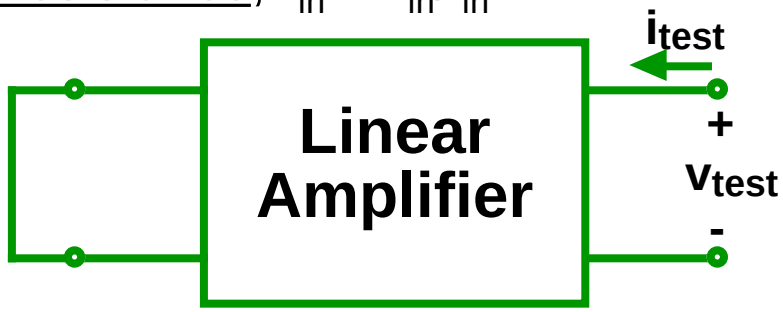
This can reduce the apparent complexity dramatically.

Linear amplifier basics: performance metrics

The characteristics of linear amplifiers that we use to compare different amplifier designs, and to judge their performance and suitability for a given application are given below:



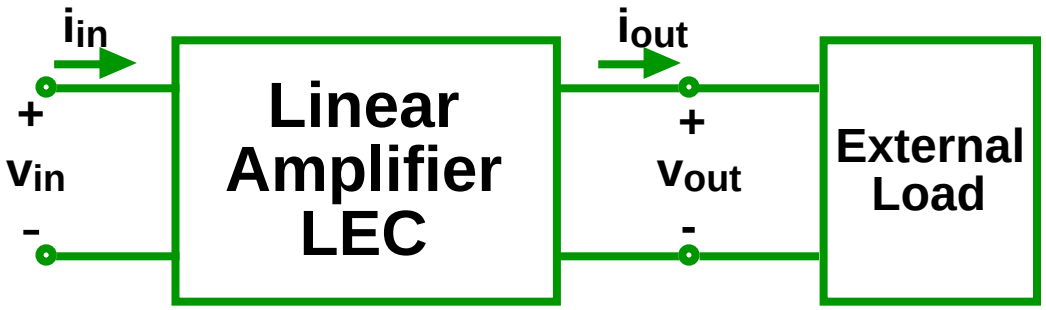
Voltage gain, $A_v = v_{out}/v_{in}$
Current gain, $A_i = i_{out}/i_{in}$
Power gain, $A_{power} = P_{out}/P_{in} = v_{out}i_{out}/v_{in}i_{in} = A_vA_i$
Input resistance, $r_{in} = v_{in}/i_{in}$



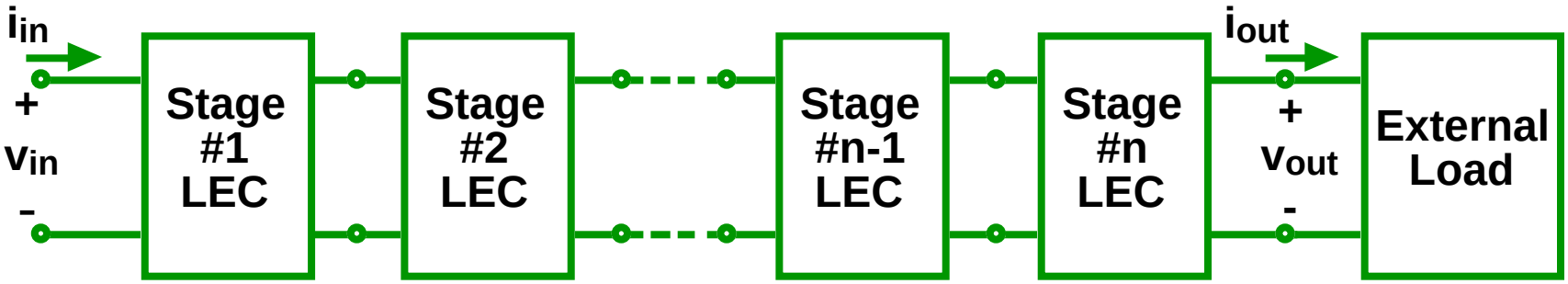
Output resistance, $r_{out} = v_{test}/i_{test}$ with $v_{in} = 0$

DC Power dissipation, $P_{DC} = (V_+ - V_-)(\Sigma I_{BIAS}\text{'s})$

Linear amplifier basics: multi-stage structure; two-ports



The typical linear amplifier is comprised of multiple building-block stages, often such as the single transistor stages we introduced on Slide 14 (and which will be the topic of Lect. 19):

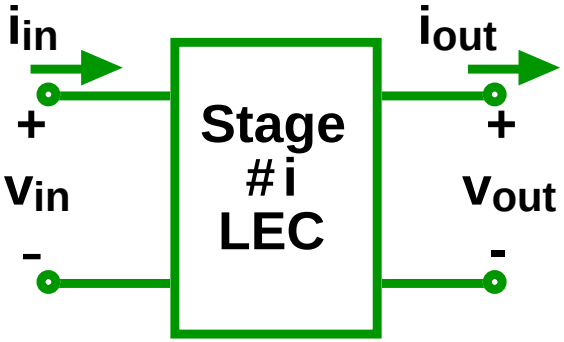


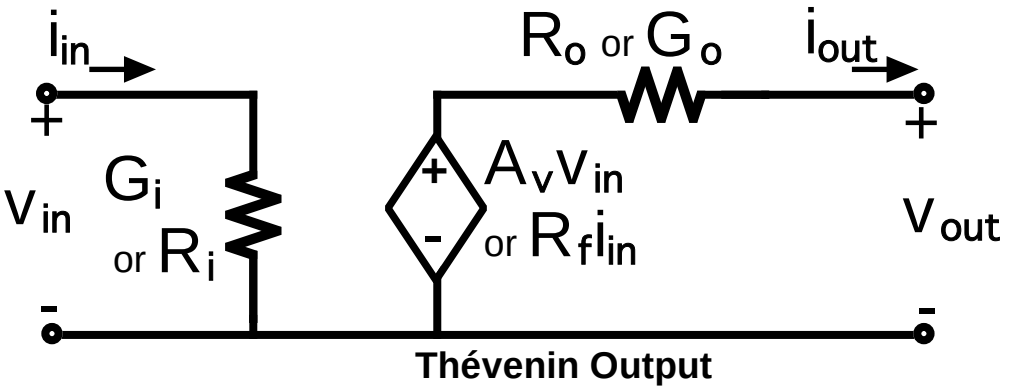
A useful concept and tool for analyzing, as well as designing, such multi-stage amplifiers is the two-port representation.

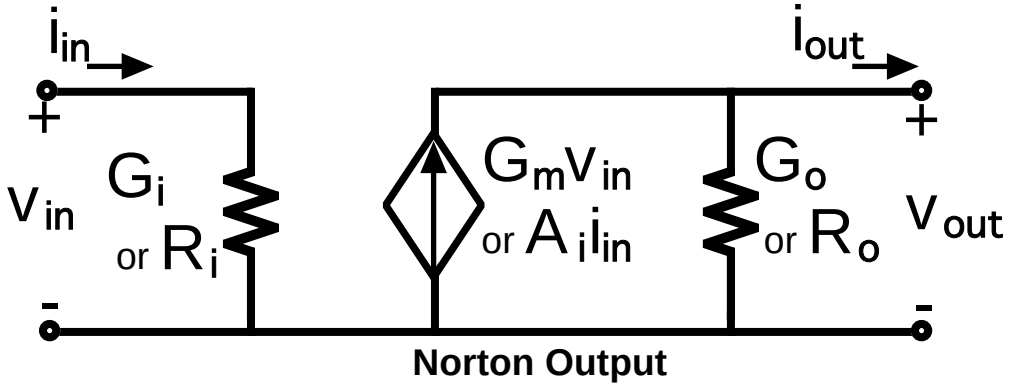
Note: More advanced multi-stage amplifiers might include feedback, the coupling of the outputs of some stages to the inputs of preceding stages. This is not shown in this figure.

Linear amplifier basics: two-port representations

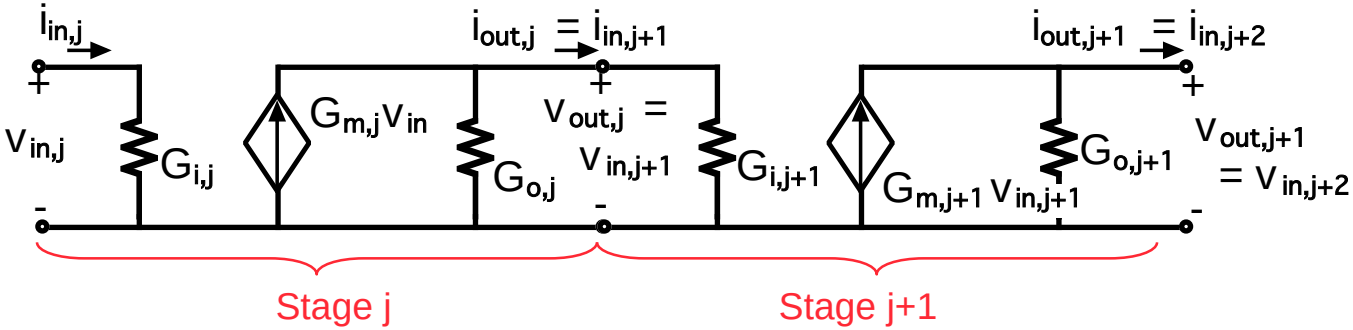
Each building block stage can be represented by a "two-port" model with either a Thévenin or a Norton equivalent at its output:







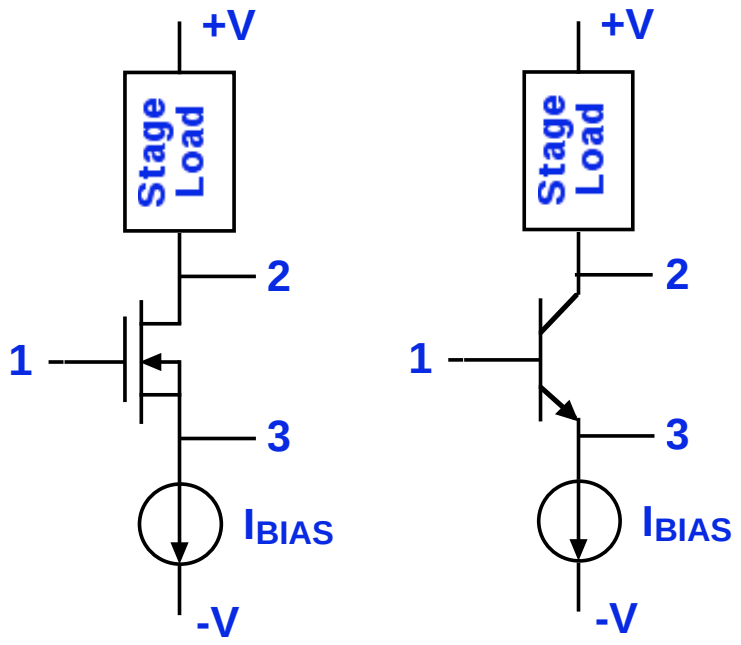
Two-ports can simplify the analysis and design of multi-stage amplifiers:



Linear amplifier layouts: The practical ways of putting inputs to, and taking outputs from, transistors to form linear amplifiers

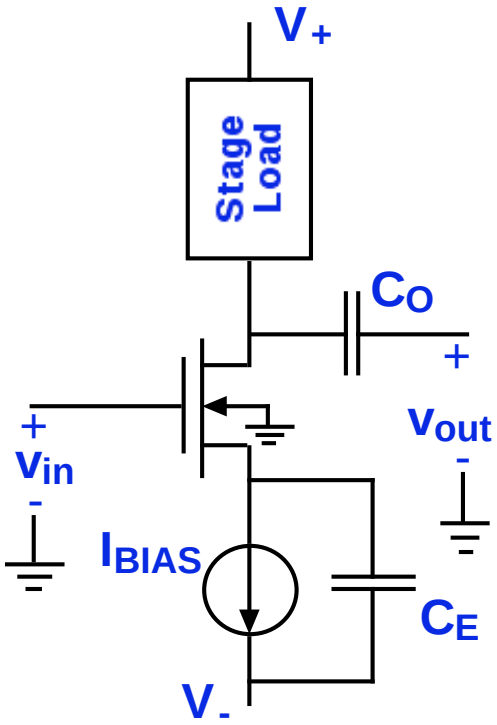
There are 12 choices: three possible nodes to connect to the input, and for each one, two nodes from which to take an output, and two choices of what to do with the remaining node (ground it or connect it to something).

Not all these choices work well, however. In fact only three do:



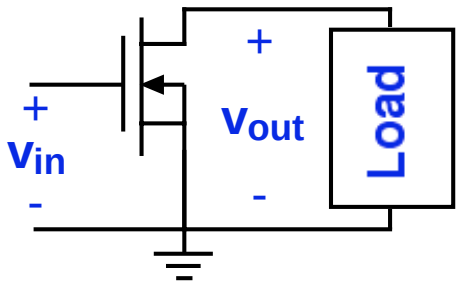
Name	Input	Output	Grounded
Common source/emitter	1	2	3
Common gate/base	3	2	1
Common drain/collector (Source/emitter follower)	1	3	2
Source/emitter degeneration	1	2	none

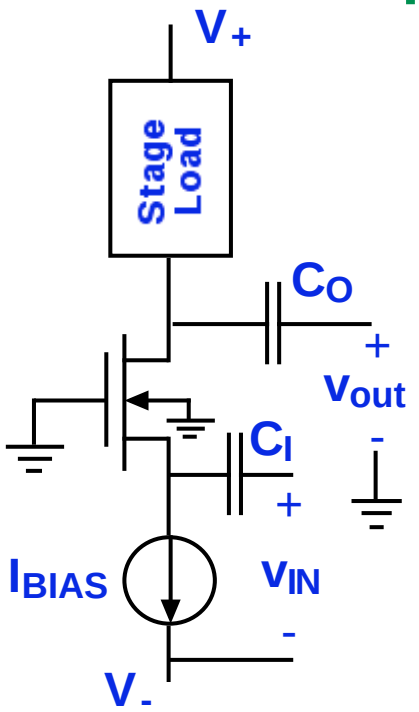
- **Three MOSFET single-transistor amplifiers**



COMMON SOURCE

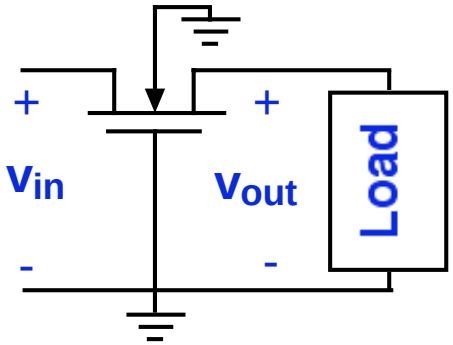
Input: gate
Output: drain
Common: source
Substrate: to source

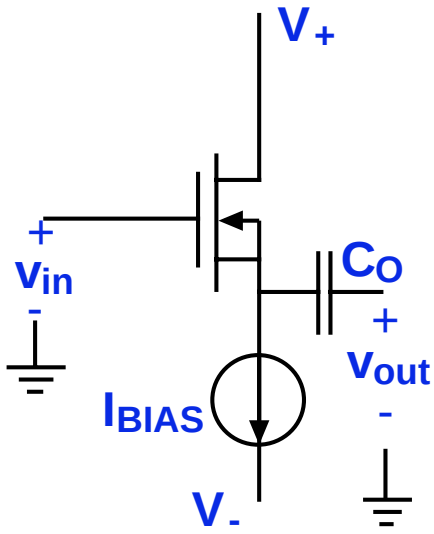




COMMON GATE

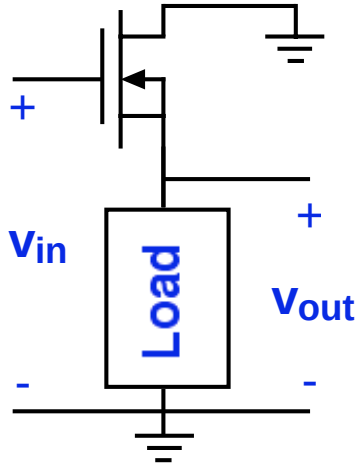
Input: source; Output: drain
Common: gate
Substrate: to ground



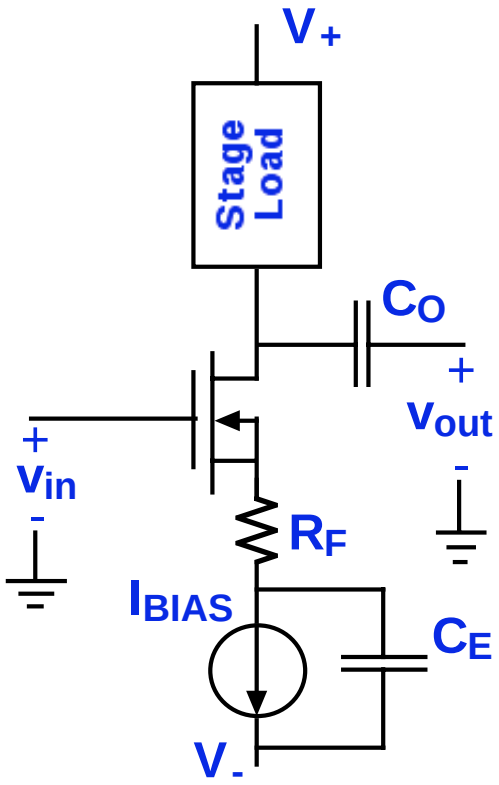


SOURCE FOLLOWER

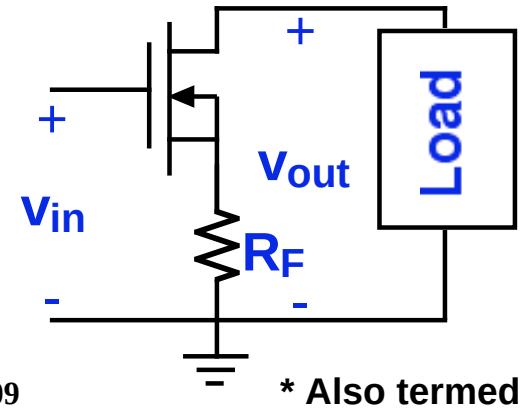
Input: gate
Output: source
Common: drain
Substrate: to source

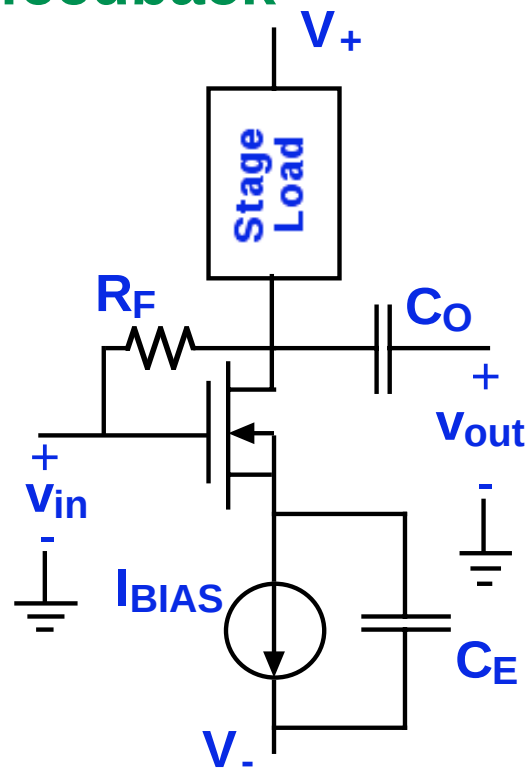


- **Single-transistor amplifiers with feedback**

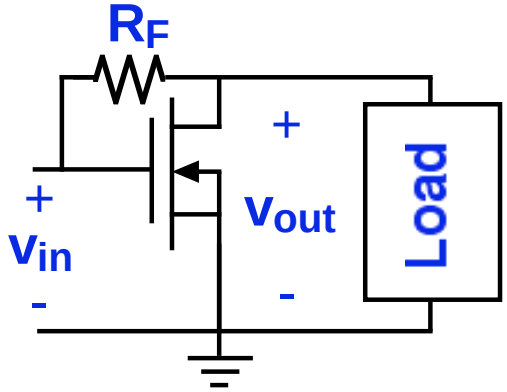


PARALLEL FEEDBACK*





SERIES FEEDBACK

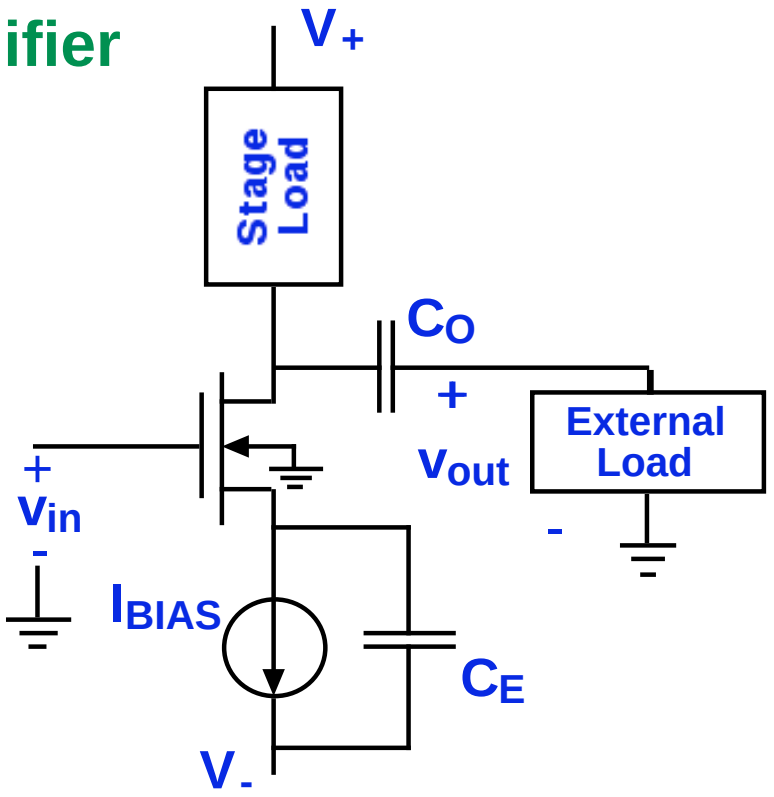


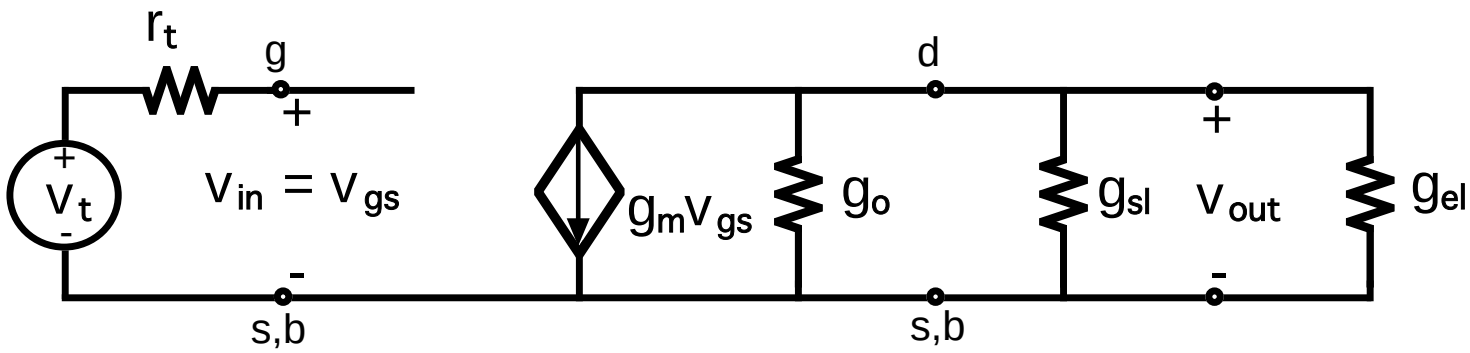
* Also termed "source degeneracy"

- **Common source amplifier**

Common source

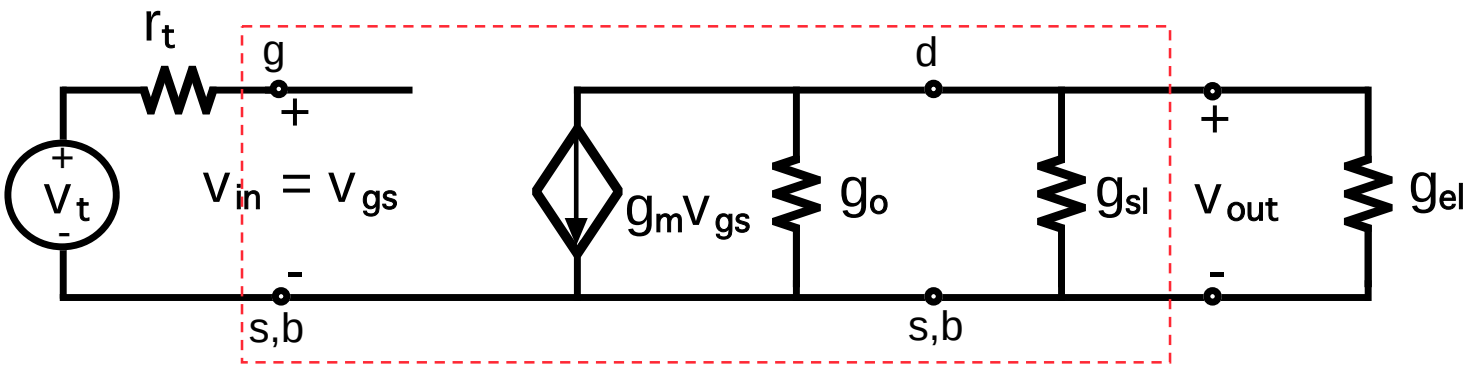
- **Input to gate**
- **Output from drain**
- **Source common to input and output, and grounded**





Mid-band LEC for common source

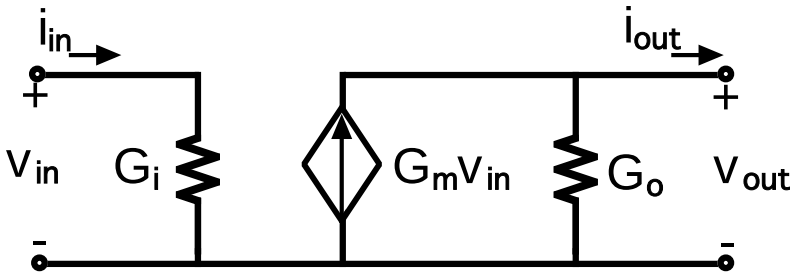
Common source amplifier, cont.

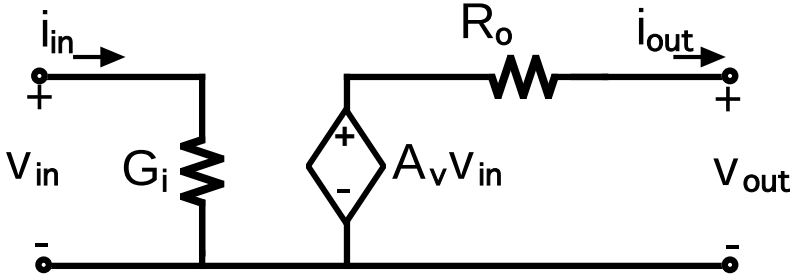


$$v_{out} = -\frac{g_m v_{in}}{g_o + g_{sl} + g_{el}} = -\frac{g_m v_t}{g_o + g_{sl} + g_{el}}$$

a large |#|

Two-ports:





$$G_i = 0 \quad (R_i = \infty)$$

$$G_o = (g_o + g_{sl})$$

$$G_m = -g_m$$

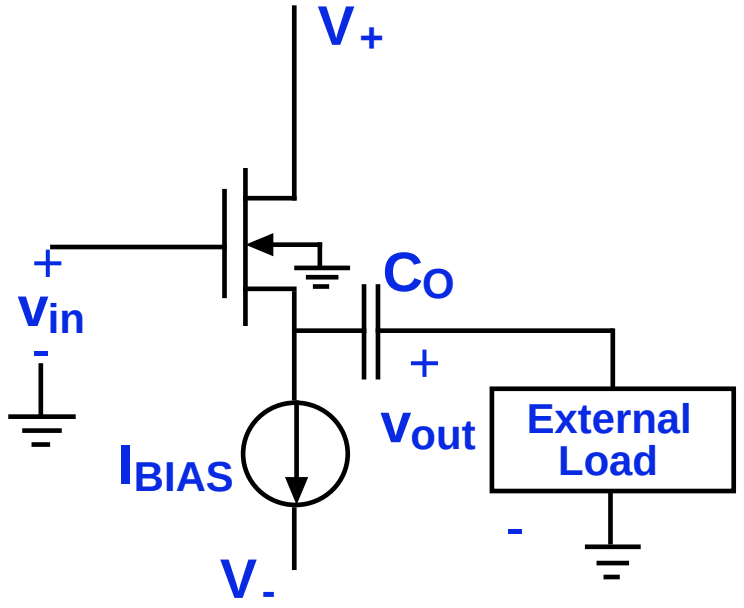
$$A_v = -\frac{g_m}{g_o + g_{sl}} \quad \left(= \frac{G_m}{G_o}\right)$$

A good workhorse gain stage

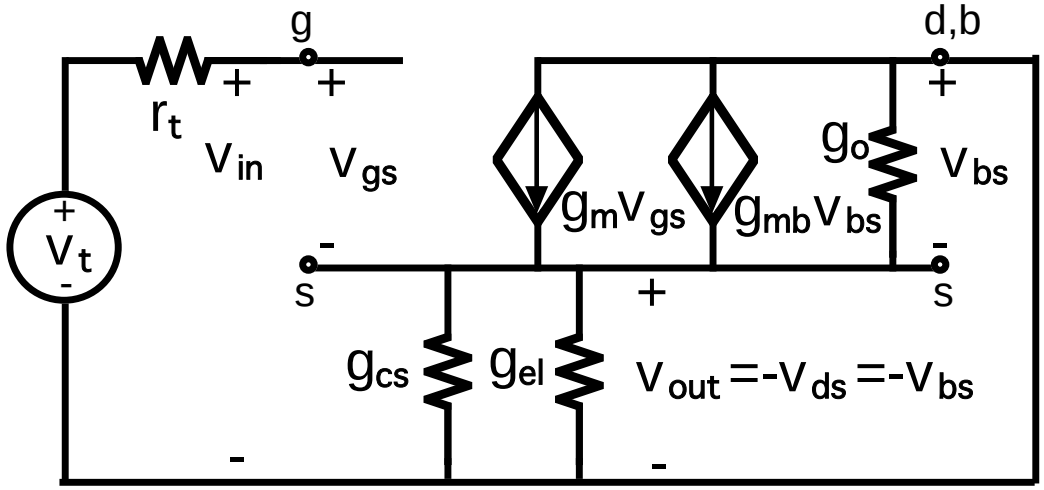
- **Source follower (common drain) amplifier**

Source Follower (Common drain)

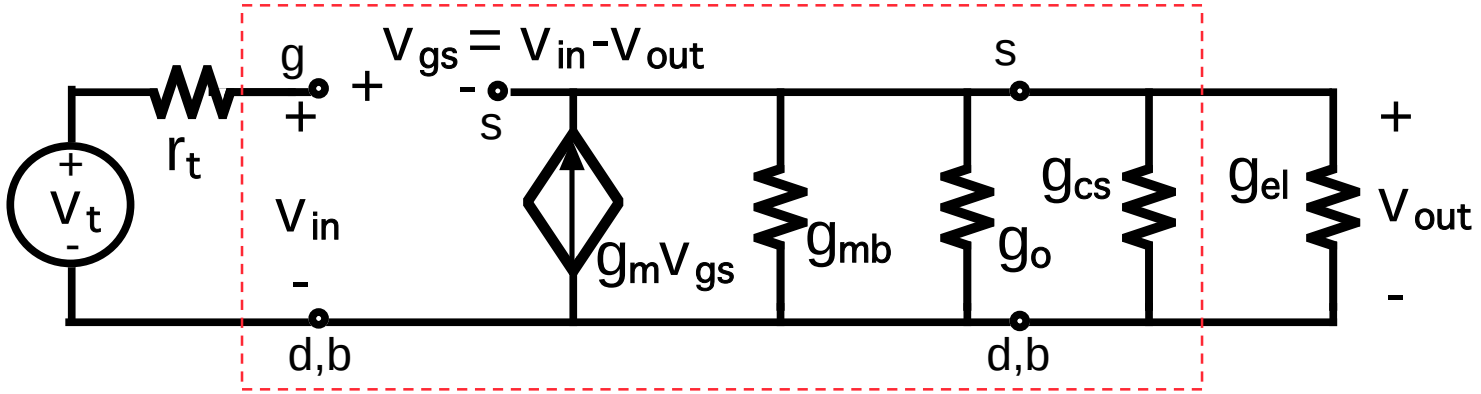
- Input to gate
- Output from source
- Drain common to input and output, and incrementally grounded



Mid-band LEC for source follower (common drain)



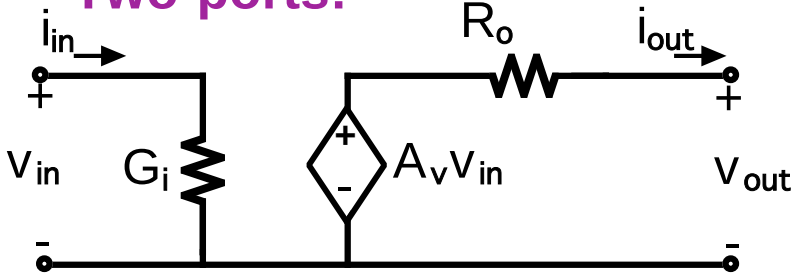
Source follower (common drain) amplifier, cont.

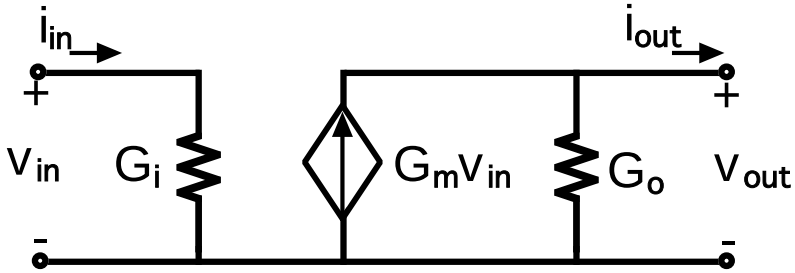


$$v_{out} = \frac{g_m(v_{in} - v_{out})}{g_{mb} + g_o + g_{cs} + g_{el}} \Rightarrow v_{out} = \frac{g_m v_{in}}{g_m + g_{mb} + g_o + g_{cs} + g_{el}} \approx \frac{g_m v_{in}}{g_m + g_{mb}} = \frac{v_{in}}{1+\eta}$$

≈ 1

Two-ports:





$$A_v \approx \frac{1}{1+\eta}$$

$$G_i = 0 \quad (R_i = \infty)$$

$$G_m = A_v G_o = g_m$$

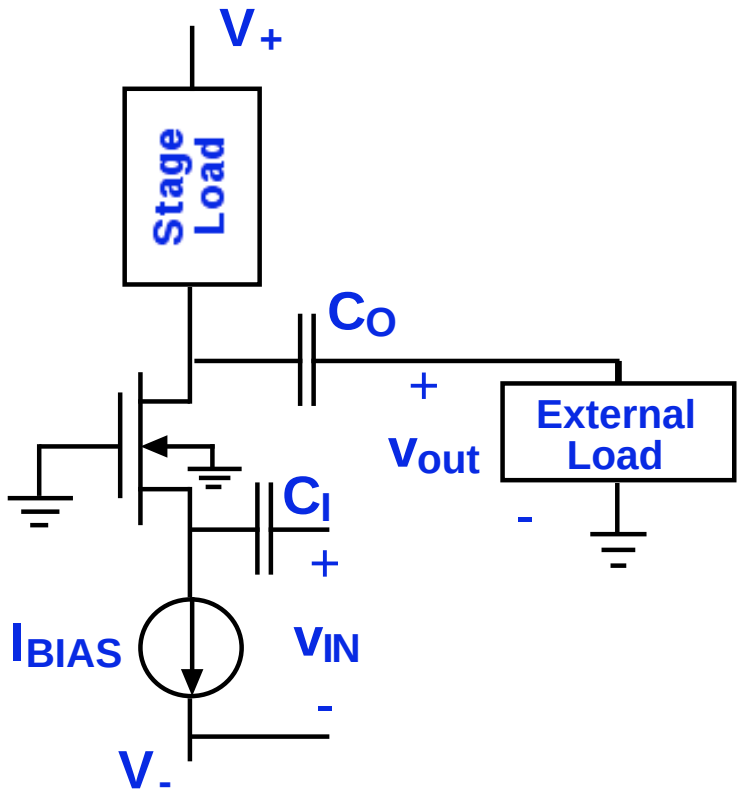
$$G_o = (g_m + g_{mb} + g_o + g_{cs}) \approx (g_m + g_{mb}) = (1+\eta) g_m$$

A great output buffer stage with small R_{out} and large R_{in}; $A_v \approx 1$, A_i large.

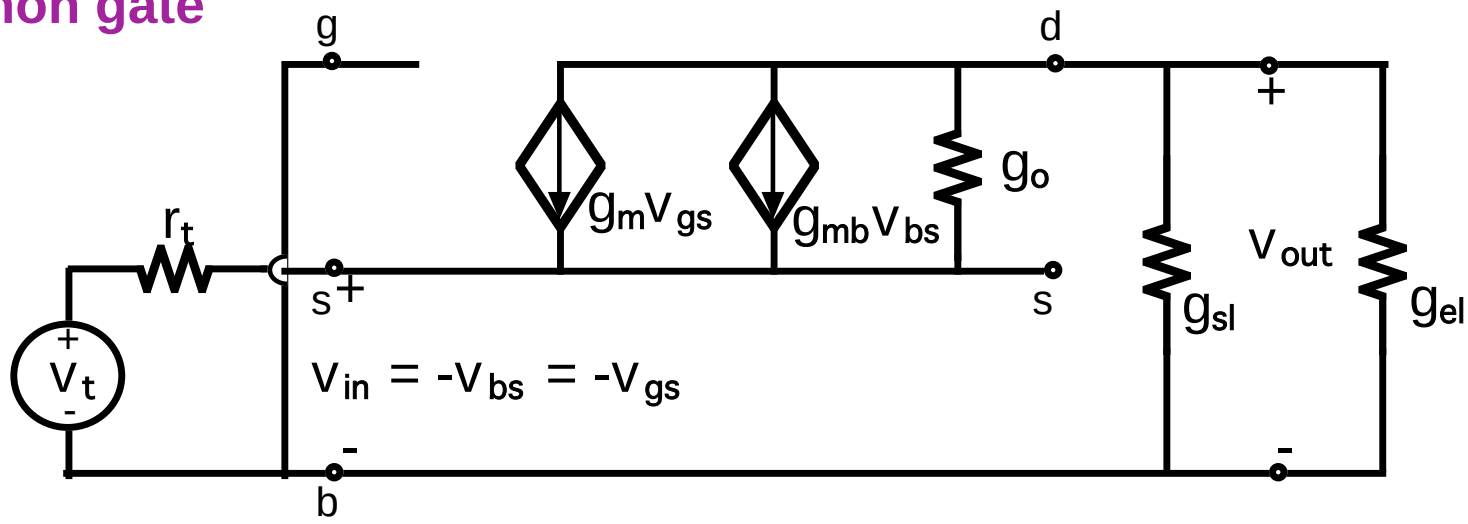
- **Common gate amplifier**

Common Gate

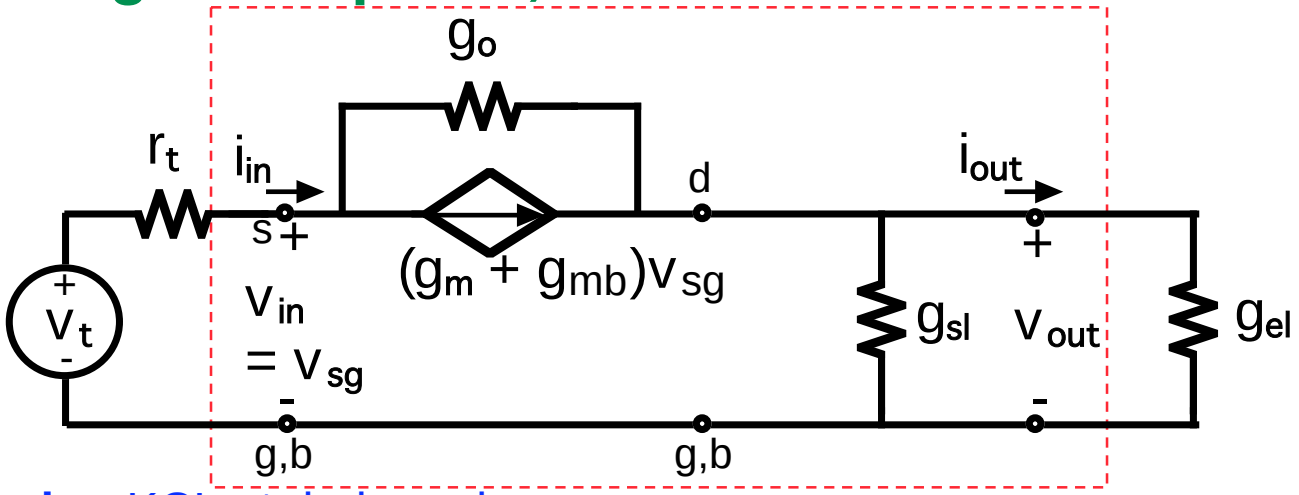
- Input to source
- Output from drain
- Gate common to input and output, and grounded



Mid-band LEC for common gate



Common gate amplifier, cont.



Voltage gain - KCL at drain node:

$$(g_m + g_{mb})v_{in} = (g_{sl} + g_{el})v_{out} + g_o(v_{out} + v_{in}) \quad \Rightarrow \quad v_{out} = \frac{(g_m + g_{mb} + g_o)v_{in}}{(g_{sl} + g_{el} + g_o)} \approx \frac{(1+\eta)g_m}{(g_{sl} + g_{el} + g_o)} v_{in}$$

a large |#|

Current gain - Current divider g_{sl}/g_{el} noting that $i_{in} = -i_d$:

$$v_{out} = \frac{i_{in}}{(g_{sl} + g_{el})} = \frac{i_{out}}{g_{el}} \quad \Rightarrow \quad i_{out} = \frac{g_{el}}{(g_{sl} + g_{el})} i_{in}$$

≈ 1 if g_{sl} small

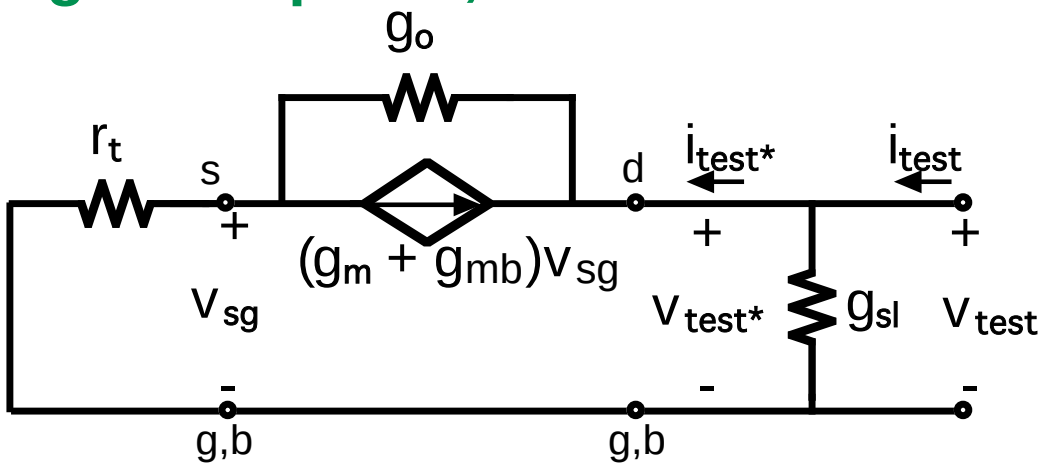
Input resistance - Use $v_{out}(i_{in})$ and $v_{out}(v_{in})$ expressions:)

$$v_{out} = \frac{i_{in}}{(g_{sl} + g_{el})}, \quad v_{out} = \frac{(g_m + g_{mb} + g_o)v_{in}}{(g_{sl} + g_{el} + g_o)} \quad \Rightarrow$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{(g_{sl} + g_{el} + g_o)}{(g_{sl} + g_{el})(g_m + g_{mb} + g_o)} \approx \frac{1}{(g_m + g_{mb})} = \frac{1}{(1+\eta)g_m}$$

small

Common gate amplifier, cont.



Output resistance - Set $v_t = 0$, and apply v_{test*} to output; find i_{test*}:

$$i_{test*} = g_o\left(v_{test*} - i_{test*}r_t\right) - \left(g_m + g_{mb}\right)i_{test*}r_t \quad \Rightarrow \quad G_o = g_{sl} + \frac{i_{test*}}{v_{test*}} = g_{sl} + \frac{g_o}{1 + r_t\left(g_m + g_{mb} + g_o\right)}$$

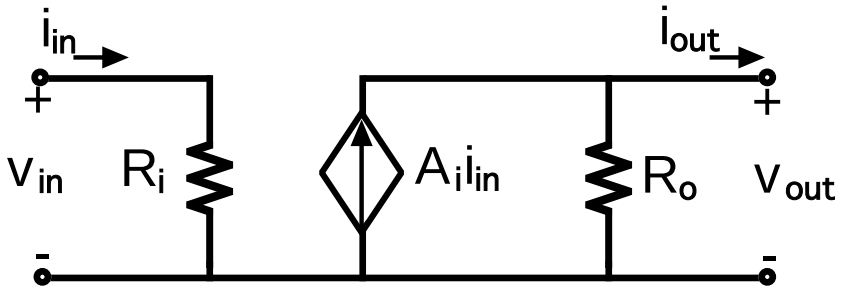
a small #

Two-port:

$$R_i \approx 1/\left(1+\eta\right)g_m \quad \left(R_i \text{ very small}\right)$$

$$A_i = g_{el}/\left(g_{el} + g_{sl}\right) \approx 1$$

$$G_o \approx g_{sl} + \frac{g_o}{1 + r_t\left(g_m + g_{mb}\right)} \quad \left(R_o \text{ very large}\right)$$



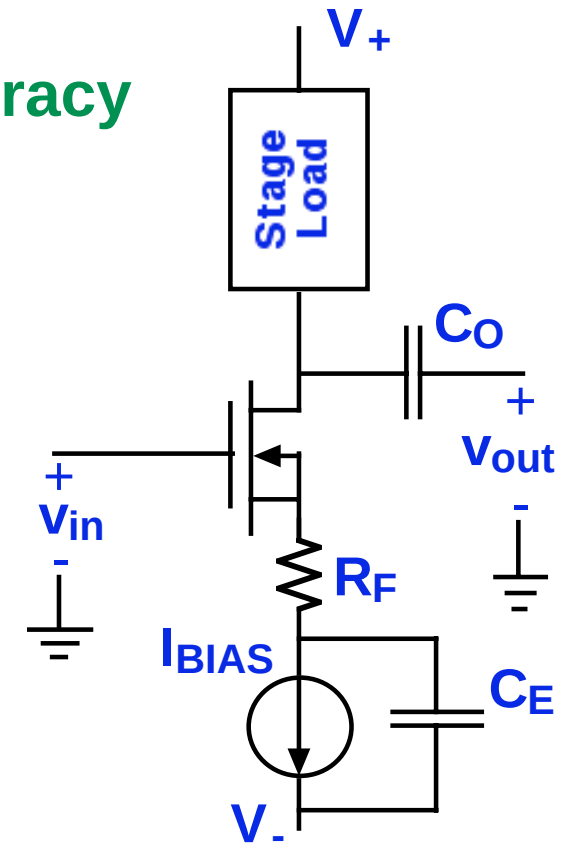
A very small R_i, very large R_o stage often used to complement other stages; $A_i \approx 1$, A_v large.

- **Series Feedback: source degeneracy**

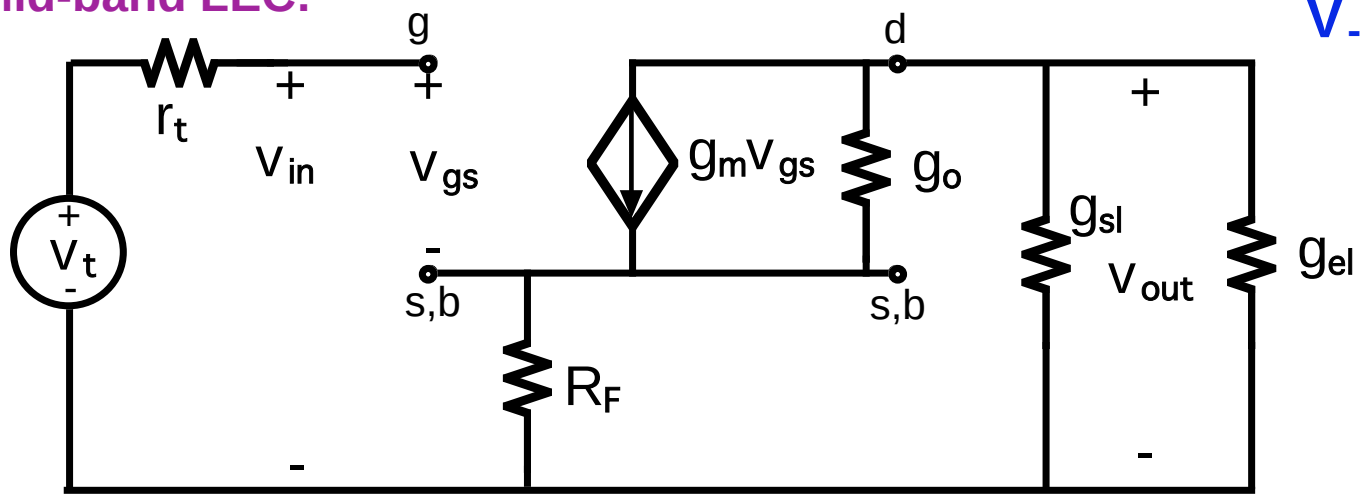
Series feedback

- **Output signal fed back to the input through a passive element that is common to the input and output circuits.**

Useful in discrete device circuit design; we use it to understand common-mode gain suppression in differential amplifiers



Mid-band LEC:



We find:

$$A_v = v_{out}/v_{in}$$

$$\approx -r_l/R_F$$

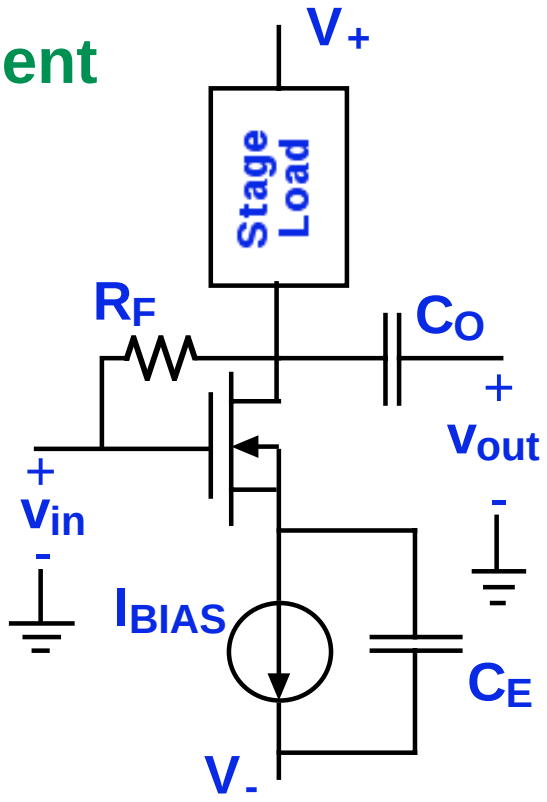
$$r_l \equiv 1/(g_{sl} + g_{el})$$

- **Feedback: shunt feedback element**

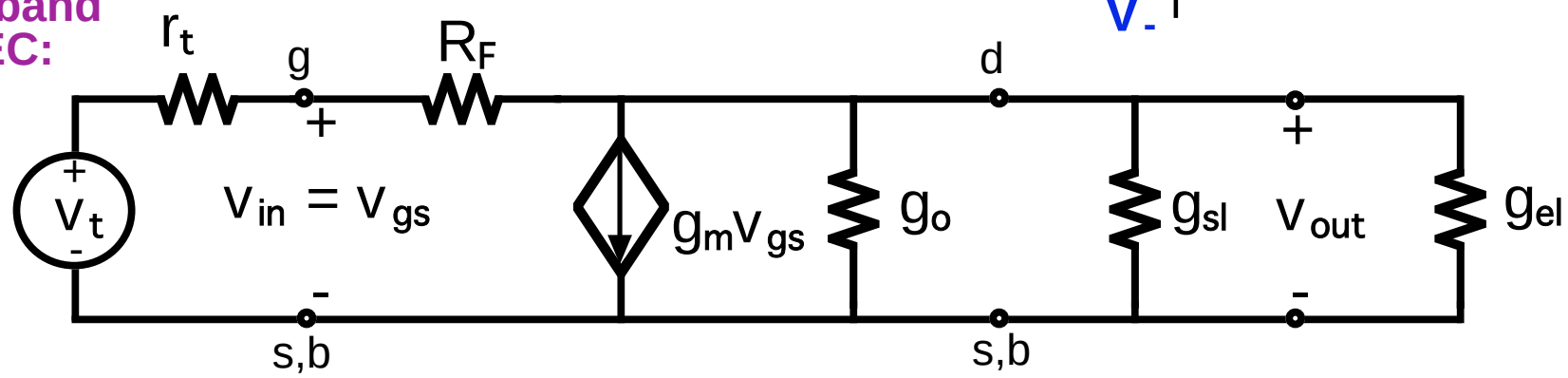
Shunt feedback

- **Output signal fed back to the input through a passive element forming a bridge between the input and output.**

Used to stabilize high gain circuits and in transimpedance amplifiers; the same topology leads to the Miller effect. (Lec 23)



Mid-band LEC:



We find: $A_v = v_{out}/v_{in} \approx -g_m R_F$

- **Summary of the single transistor stages (MOSFET)**

MOSFET	Voltage gain, A_v	Current gain, A_i	Input resistance, R_i	Output resistance, R_o
Common source	$-\frac{g_m}{[g_o + g_l]} \left(= -g_m r_l^{'}\right)$	∞	∞	$r_o \left(= \frac{1}{g_o}\right)$
Common gate	$\approx [g_m + g_{mb}]\, r_l^{'}$	≈ 1	$\approx \frac{1}{[g_m + g_{mb}]}$	$\approx r_o \left\{1 + \frac{[g_m + g_{mb} + g_o]}{g_t}\right\}$
Source follower	$\frac{[g_m]}{[g_m + g_{mb} + g_o + g_l]} \approx 1$	∞	∞	$\frac{1}{[g_m + g_o + g_l]} \approx \frac{1}{g_m}$
Source degeneracy (series feedback)	$\approx -\frac{r_l}{R_F}$	∞	∞	$\approx r_o$
Shunt feedback	$-\frac{[g_m - G_F]}{[g_o + G_F]} \approx -g_m R_F$	$-\frac{g_l}{G_F}$	$\frac{1}{G_F[1 - A_v]}$	$r_o \,\|\|\, R_F \left(= \frac{1}{[g_o + G_F]}\right)$

Power gain, $A_p = A_v \cdot A_i$

Note: When $v_{bs} = 0$ the g_{mb} factors should be deleted.

Lecture 18 - Single Transistor Amplifier Stages - Summary

- **Amplifier Building-blocks - single transistor stages**

  Common source: good voltage and current gain
  large R_{in} and R_{out}
  good gain stage

  Common gate: very small R_{in}; very large R_{out}
  unity current gain; good voltage gain
  will find paired with other stages to form "cascode"

  Source follower: very small R_{out}; very large R_{in}
  unity voltage gain; good current gain
  an excellent output stage or buffer

  Series feedback: moderate voltage gain dependant on resistor ratio

  Shunt feedback: used in transimpedance amplifiers

6.012 Microelectronic Devices and Circuits

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