6.012 - Microelectronic Devices and Circuits

Lecture 13 - Linear Equivalent Circuits - Outline

- **Announcements**
  Exam Two - Coming next week, Nov. 5, 7:30-9:30 p.m.
- **Review - Sub-threshold operation of MOSFETs**
- **Review - Large signal models, w. charge stores**
  p-n diode, BJT, MOSFET (sub-threshold and strong inversion)
- **Small signal models; linear equivalent circuits**
  General two, three, and four terminal devices

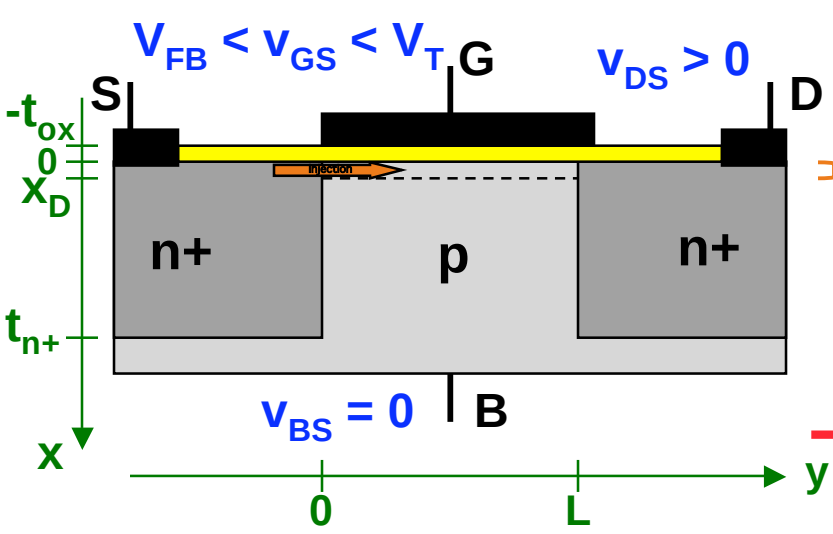
  pn diodes: Linearizing the exponential diode
  Adding linearized charge stores

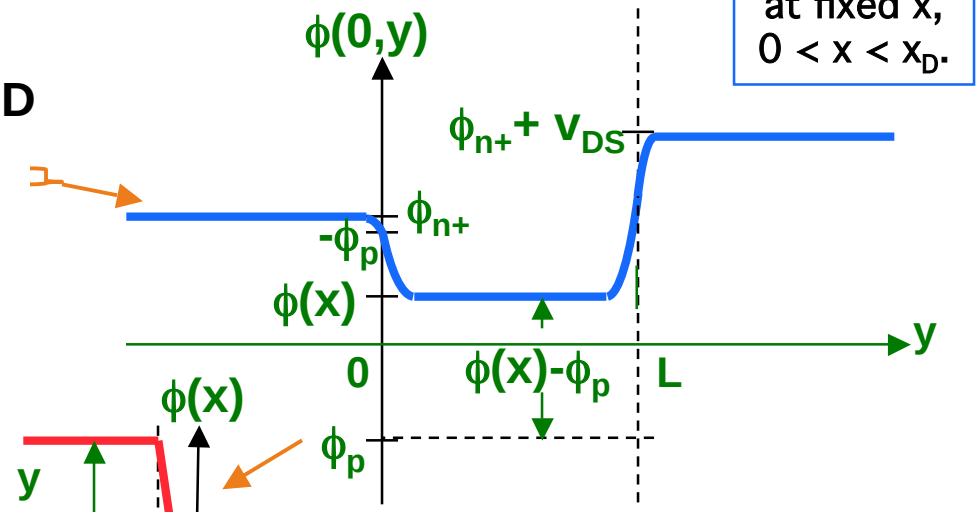
  BJTs: Linearizing the F.A.R. β-model
  Adding linearized charge stores

  MOSFETs: Linearized strong inversion model
  Linearized sub-threshold model
  Adding linearized charge stores

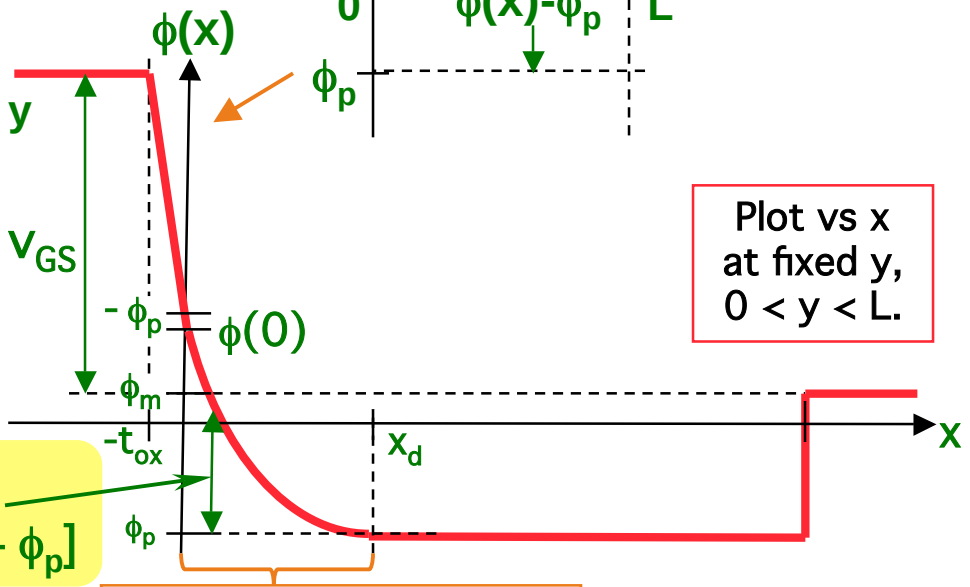
Sub-threshold Operation of MOSFETs, cont.

- The barrier at the n^+-p junction is lowered near the oxide-Si interface for any $v_{GS} > V_{FB}$.
- The barrier is lowered by $\phi(x) - \phi_p$ for $0 < x < x_D$.
  (This is the effective v_{BE} on the lateral BJT between x and x + dx.)





Plot vs y at fixed x, $0 < x < x_D$.



Plot vs x at fixed y, $0 < y < L$.

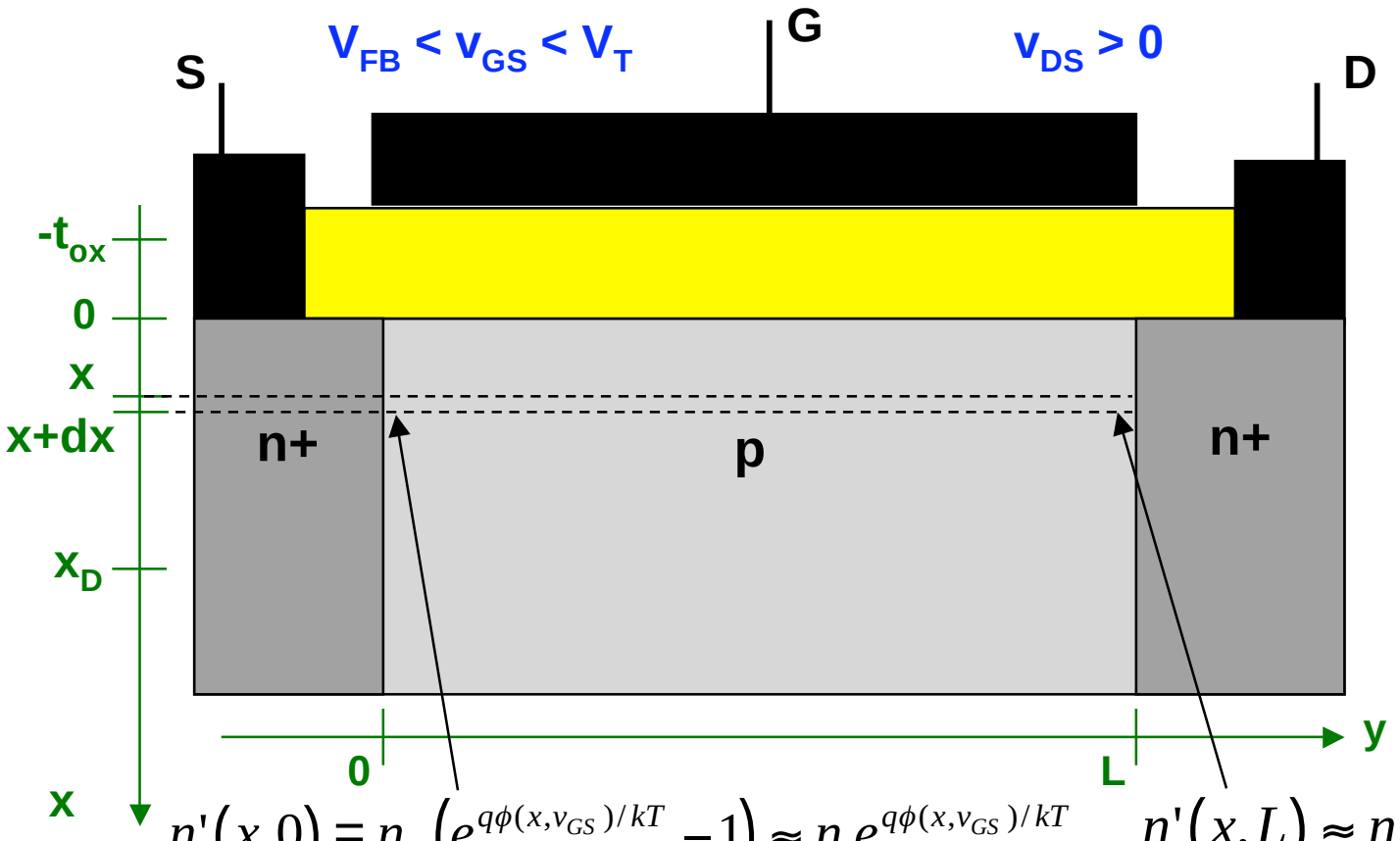
- The barrier lowering (effective forward bias) (1) is controlled by v_{GS}, and (2) decreases quickly with x.

$v_{BE,eff}(x) = [\phi(x) - \phi_p]$

Injection occurs over this range, but is largest near x = 0.

Sub-threshold Operation of MOSFETs, cont.

- To calculate i_D, we first find the current in each dx thick slab:



$$n'(x,0) = n_i\left(e^{q\phi(x,v_{GS})/kT} - 1\right) \approx n_i e^{q\phi(x,v_{GS})/kT} \qquad n'(x,L) \approx n'(x,0)\,e^{-qv_{DS}/kT}$$

$$di_D(x) = qD_e\frac{n'(x,0)-n'(x,L)}{L}\,W\,dx \approx \frac{W}{L}D_e\,q\,n_i\left(1-e^{-qv_{DS}/kT}\right)e^{q\phi(x,v_{GS})/kT}\,dx$$

Sub-threshold Operation of MOSFETs, cont.

- Integrating this from x = 0 to x = x_D using the approximate value for the integral derived in Lecture 9, and approximating the relationship between $\Delta\phi(0)$ and Δv_{GS} as linear, i.e. $\Delta\phi(0) \approx \Delta v_{GS}/n$, we arrived at:

$$i_{D,s-t}(v_{GS},v_{DS},0) \approx \frac{W}{L}\mu_e\, C_{ox}^* \left(\frac{kT}{q}\right)^2 [n-1]\; e^{q\{v_{GS}-V_T\}/nkT}\left(1-e^{-qv_{DS}/kT}\right)$$

where $$n \approx \left\{1+\frac{1}{C_{ox}^*}\sqrt{\frac{\varepsilon_{Si}qN_A}{2[-2\phi_p]}}\right\} = \alpha$$

Variations on this form:

It is common to see $i_{D,s-t}$ written using the factors K and γ we defined earlier, and with kT/q replaced by V_t, the thermal voltage, and $[n\text{ -}1]$ replaced in the pre-factor. Written this way, we have:

$$i_{D,s-t}(v_{GS},v_{DS},0) \approx K\, V_t^2\, \frac{\gamma}{2\sqrt{[-2\phi_p]}}\; e^{\{v_{GS}-V_T\}/nV_t}\left(1-e^{-v_{DS}/V_t}\right)$$

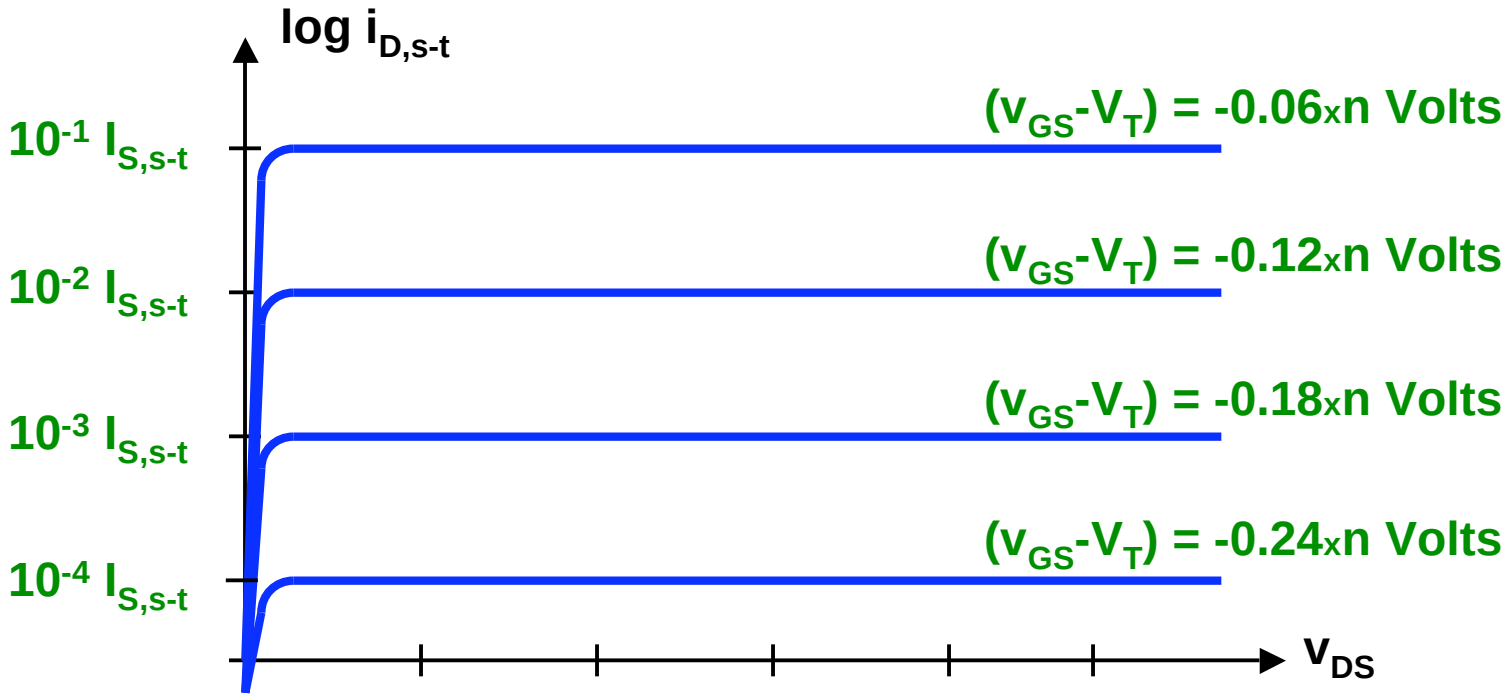
with

$$\gamma \equiv \frac{\sqrt{2\varepsilon_{Si}qN_A}}{C_{ox}^*}, \quad K \equiv \frac{W}{L}\mu_e C_{ox}^*, \quad n(v_{BS}) \approx \left\{1+\frac{\gamma}{2\sqrt{[-2\phi_p - v_{BS}]}}\right\}$$

Sub-threshold Output Characteristic

- We plot a family of i_D vs v_{DS} curves with (v_{GS} - V_T) as the family variable, after first defining the sub-threshold diode saturation current, $I_{S,s-t}$:

$$I_{S,s-t} \equiv K V_t^2 \frac{\gamma}{2\sqrt{[-2\phi_p]}} = K V_t^2 [n-1]$$

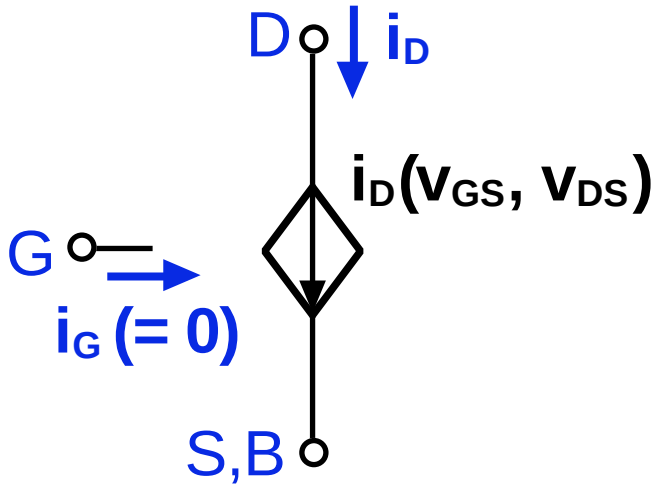


$$i_{D,s-t}(v_{GS}, v_{DS}, 0) \approx I_{S,s-t} e^{\{v_{GS}-V_T\}/nV_t} \left(1 - e^{-v_{DS}/V_t}\right)$$

Large Signal Model for MOSFET Operating Sub-threshold

- **The large signal model for a MOSFET operating in the weak inversion or sub-threshold region looks the same model as that for a device operating in strong inversion ($v_{GS} > V_T$) EXCEPT there is a different equation relating i_D to v_{GS}, v_{DS}, and v_{BS}:**

We will limit our model to $v_{GS} \le V_T, v_{DS} > 3V_t$ **and** $v_{BS} = 0.$

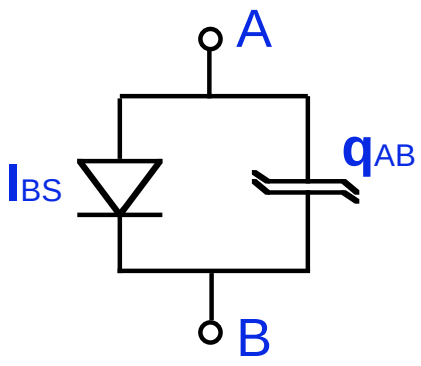


$$i_{G,s-t}(v_{GS}, v_{DS}, v_{BS}) = 0$$

$$i_{D,s-t}(v_{GS}, v_{DS}, 0) \approx I_{S,s-t}\underbrace{(1-\lambda v_{DS})}_{\text{Early effect}} e^{\{v_{GS}-V_{To}\}/nV_t} \underbrace{\cancel{\left(1-e^{-v_{DS}/V_t}\right)}}_{\approx 1 \text{ for } v_{DS} > 3V_t}$$

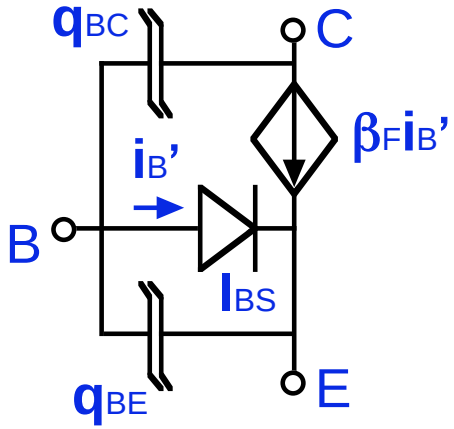
Large signal models with charge stores:

p-n diode:



q_{AB}: Excess carriers on p-side plus excess carriers on n-side plus junction depletion charge.

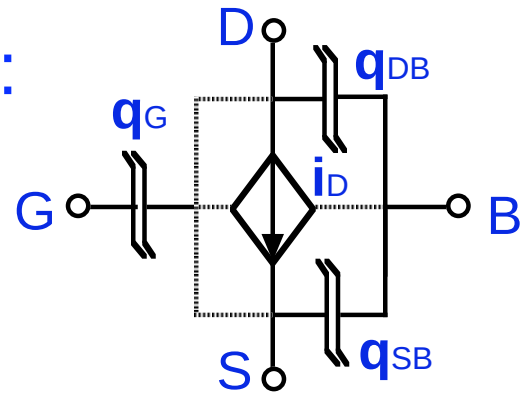
BJT: npn
(in F.A.R.)



q_{BE}: Excess carriers in base plus E-B junction depletion charge

q_{BC}: C-B junction depletion charge

MOSFET:
n-channel



q_G: Gate charge; a function of v_{GS}, v_{DS}, and v_{BS}.

q_{DB}: D-B junction depletion charge

q_{SB}: S-B junction depletion charge

Signal notation:

A transistor circuit, whether digital or analog, is typically connected to several DC power supplies that establish the desired DC "bias" currents and voltages throughout it. It also typically has one or more time varying input signals that result in time varying currents and voltages (one of which is the desired output of the circuit) being added to the DC bias currents and voltages.

Each voltage and current in such a circuit thus has a DC bias portion and a signal portion, which add to make the total. We use the following notation to identify these components and the total:

$$i_A(t) = I_A + i_a(t)$$

$$v_{AB}(t) = V_{AB} + v_{ab}(t)$$

Total: lower-case letter and upper-case subscript.

Bias: upper-case letter and subscript.

Signal: lower-case letter and subscript.

DC Bias Values:

To construct linear amplifiers and other linear signal processing circuits from non-linear electronic devices we must use regions in the non-linear characteristics that are locally linear over useful current and voltage ranges, and operate there.

To accomplish this we must design the circuit so that the DC voltages and currents throughout it "bias" all the devices in the circuit into their desired regions, e.g. yield the proper bias currents and voltages:

$$I_A, I_B, I_C, I_D, \text{etc.} \quad \text{and} \quad V_{AG}, V_{BG}, V_{CG}, V_{DG}, \text{etc.}$$

This design is done with the signal inputs set to zero and using the large signal static device models we have developed for the non-linear devices we studied: diodes, BJTs, MOSFETs.

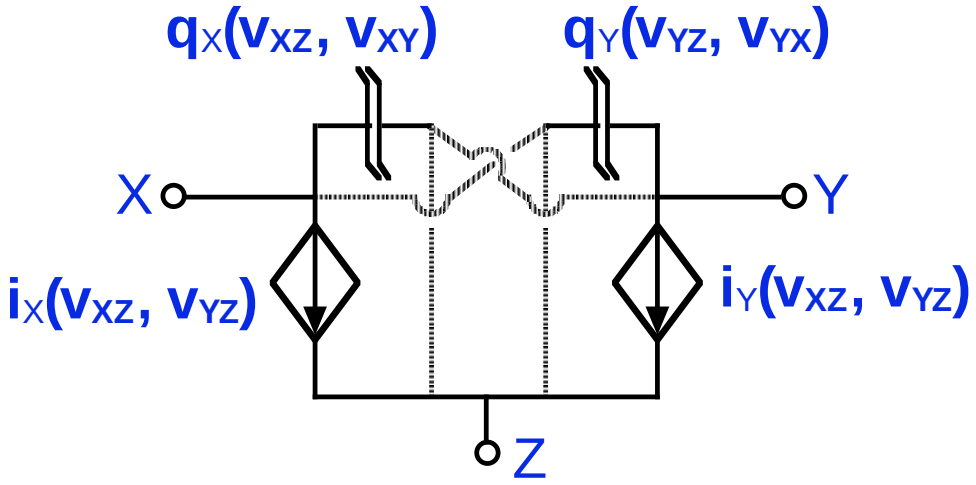
Working with these models to get the bias values, though not onerous, can be tedious. It is not something we want to have to do to find voltages and currents when the signal inputs are applied. Instead we use linear equivalent circuits .

Linear equivalent circuits:

- After biasing each non-linear devices at the proper point the signal currents and voltages throughout the circuit will be linearly related for small enough input signals. To calculate how they are related, we make use of the linear equivalent circuit (LEC) of our circuit.
- The LEC of any circuit is a combination of linear circuit elements (resistors, capacitors, inductors, and dependent sources) that correctly models and predicts the first-order changes in the currents and voltages throughout the circuit when the input signals change.
- A circuit model that represents the proper first order linear relationships between the signal currents and voltages in a non-linear device is call an LEC for that device.
- Our next objective is to develop LECs for each of the non-linear devices we have studied: diodes, BJTs biased in their forward active region (FAR), and MOSFETs biased in their sub-threshold and strong inversion FARs.

Creating a linear equivalent circuit, LEC:

Consider a device with three terminals, X, Y, and Z:



Suppose, as is our situation with the large signal device models we have developed in 6.012, that we have expressions for the currents into terminals X and Y in terms of the voltages v_{XZ} and v_{YZ}:

$$i_X(v_{XZ}, v_{YZ}) \quad \text{and} \quad i_Y(v_{XZ}, v_{YZ})$$

and that we similarly have expressions for the charge stores associated with terminals X and Y:

$$q_X(v_{XZ}, v_{YZ}) \quad \text{and} \quad q_Y(v_{XZ}, v_{YZ})$$

Creating an LEC, cont.:

We begin with our static model expressions for the terminal characteristics, and write a Taylor's series expansion of them about a bias point, Q, defined as a specific set of v_{XZ} and v_{YZ} that we write, using our notation, as V_{XZ} and V_{YZ}

For example, for the current into terminal X we have:

$$i_X(v_{XZ},v_{YZ}) = i_X(V_{XZ},V_{YZ}) + \left.\frac{\partial i_X}{\partial v_{XZ}}\right|_Q (v_{XZ}-V_{XZ}) + \left.\frac{\partial i_X}{\partial v_{YZ}}\right|_Q (v_{YZ}-V_{YZ}) + \frac{1}{2}\left.\frac{\partial^2 i_X}{\partial v_{XZ}^2}\right|_Q (v_{XZ}-V_{XZ})^2$$

$$+ \frac{1}{2}\left.\frac{\partial^2 i_X}{\partial v_{YZ}^2}\right|_Q (v_{YZ}-V_{YZ})^2 + \frac{1}{2}\left.\frac{\partial^2 i_X}{\partial v_{XZ}\partial v_{YZ}}\right|_Q (v_{XZ}-V_{XZ})(v_{YZ}-V_{YZ}) + \text{even higher order terms}$$

For sufficiently small* (v_{XZ}-V_{XZ}) and (v_{YZ}-V_{YZ}), the second and higher order terms are negligible, and we have:

$$i_X(v_{XZ},v_{YZ}) \approx \underbrace{i_X(V_{XZ},V_{YZ})}_{i_X(V_{XZ},V_{YZ}) = I_X(V_{XZ},V_{YZ})} + \left.\frac{\partial i_X}{\partial v_{XZ}}\right|_Q \underbrace{(v_{XZ}-V_{XZ})}_{[v_{XZ}-V_{XZ}]\equiv v_{xz}} + \left.\frac{\partial i_X}{\partial v_{YZ}}\right|_Q \underbrace{(v_{YZ}-V_{YZ})}_{[v_{YZ}-V_{YZ}]\equiv v_{yz}}$$

* What is "sufficiently small" is determined by the magnitude of the higher order derivatives.

Creating an LEC, cont.:

So far we have:

$$\underbrace{i_X(v_{XZ},v_{YZ}) - I_X(V_{XZ},V_{YZ})}_{} \approx \left.\frac{\partial i_X}{\partial v_{XZ}}\right|_Q v_{xz} + \left.\frac{\partial i_X}{\partial v_{YZ}}\right|_Q v_{yz}$$

Next we define:

$$[i_X - I_X] \equiv i_x \qquad \left.\frac{\partial i_X}{\partial v_{XZ}}\right|_Q \equiv g_i \qquad \left.\frac{\partial i_X}{\partial v_{YZ}}\right|_Q \equiv g_r$$

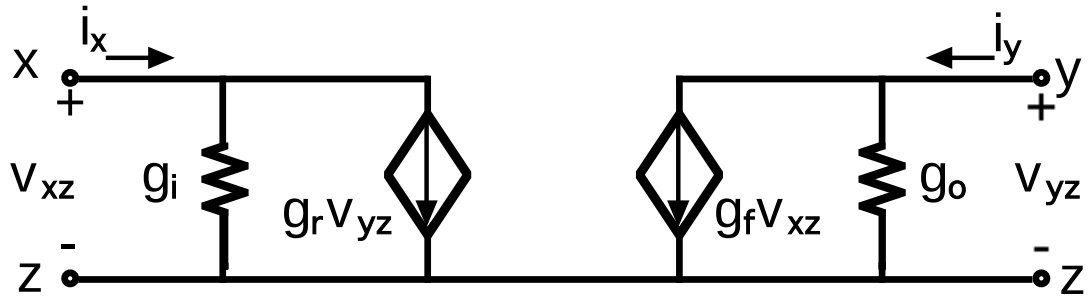
Replacing the partial derivatives with the conductances we have defined, gives us our working form of the linear equation relating the incremental variables:

$$i_x \approx g_i v_{xz} + g_r v_{yz}$$

Doing the same for i_Y, we arrive at

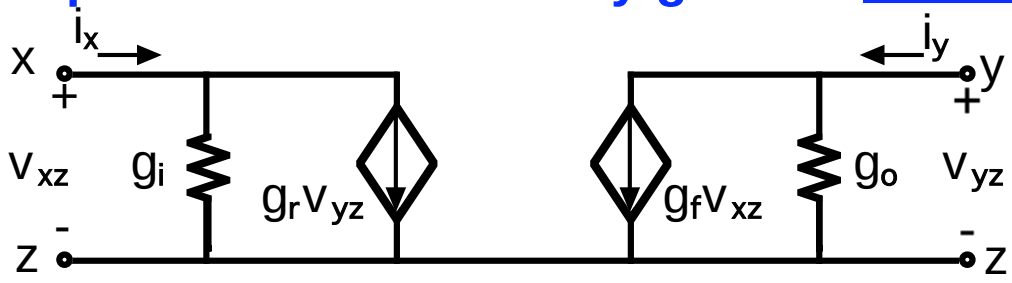
$$i_y \approx g_f v_{xz} + g_o v_{yz} \quad \text{where} \quad g_f \equiv \left.\frac{\partial i_Y}{\partial v_{XZ}}\right|_Q \qquad g_o \equiv \left.\frac{\partial i_Y}{\partial v_{YZ}}\right|_Q$$

A circuit matching these relationships is seen below:

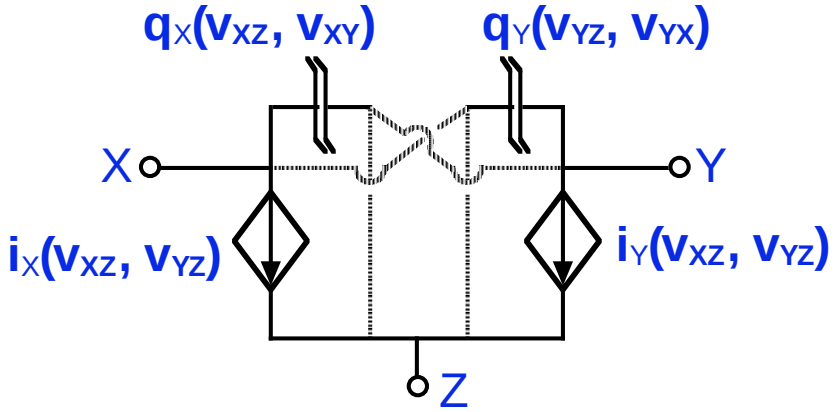


Creating an LEC, cont.:

This linear equivalent circuit is only good at low frequencies:



To handle high frequency signals, we linearize the charge stores' dependencies on voltage also.

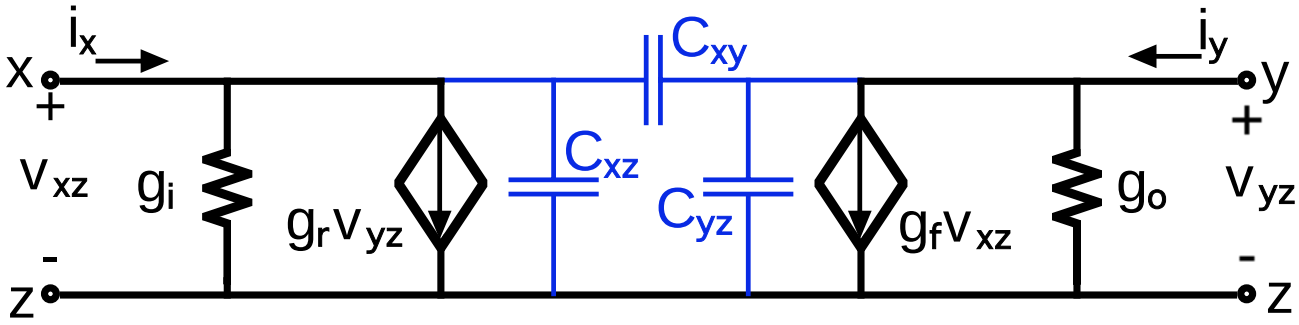


Their LECs are linear capacitors:

$$\left.\frac{\partial q_X}{\partial v_{XZ}}\right|_Q \equiv C_{xz} \qquad \left.\frac{\partial q_Y}{\partial v_{YZ}}\right|_Q \equiv C_{yz} \qquad \left.\frac{\partial q_X}{\partial v_{XY}}\right|_Q \equiv C_{xy} \left(= \left.\frac{\partial q_Y}{\partial v_{YX}}\right|_Q \right)$$

Creating an LEC, cont.:

Adding these to the model yields:



Two important points:

#1 - All of the elements in this LEC depend on the bias point, Q:

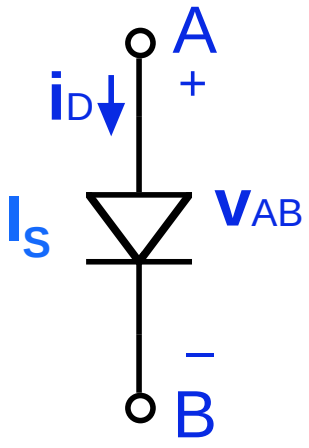
$$g_i = \left.\frac{\partial i_X}{\partial v_{XZ}}\right|_Q,\ g_r = \left.\frac{\partial i_X}{\partial v_{YZ}}\right|_Q,\ g_f = \left.\frac{\partial i_Y}{\partial v_{XZ}}\right|_Q,\ g_o = \left.\frac{\partial i_Y}{\partial v_{YZ}}\right|_Q,\ C_{xz} = \left.\frac{\partial q_X}{\partial v_{XZ}}\right|_Q,\ C_{xy} = \left.\frac{\partial q_X}{\partial v_{XY}}\right|_Q,\ C_{yz} = \left.\frac{\partial q_Y}{\partial v_{YZ}}\right|_Q$$

#2 - The device-specific nature of an LEC is manifested in the dependences of the element values on the bias currents and voltages, rather than in the topology of the LEC. Thus, different devices may have LECs that look the same. (For example, the BJ and FET LECs may look similar, but some of the elements depend much differently on the bias point values.)

Linear equivalent circuit (LEC) for p-n diodes (low f):

We begin with the static model for the terminal characteristics:

$$i_D(v_{AB}) = I_S\left[e^{qv_{AB}/kT} - 1\right]$$



Linearizing i_D about V_{AB}, which we will denote by Q (for quiescent bias point):

$$i_D(v_{AB}) \approx i_D(V_{AB}) + \left.\frac{\partial i_D}{\partial v_{AB}}\right|_Q \left[v_{AB} - V_{AB}\right]$$

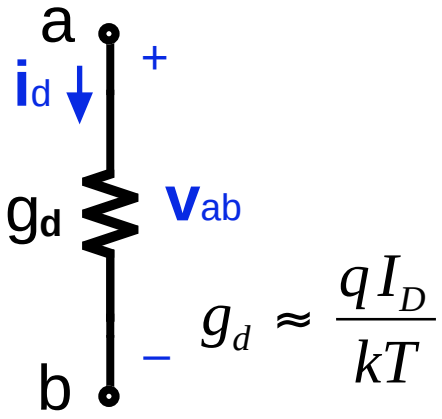
We define the equivalent incremental conductance of the diode, g_d,

$$g_d \equiv \left.\frac{\partial i_D}{\partial v_{AB}}\right|_Q = \frac{q}{kT} I_S\, e^{qV_{AB}/kT} \approx \frac{qI_D}{kT}$$

and we use our notation to write:

$$I_D = i_D(V_{AB}), \qquad i_d = \left[i_D - I_D\right], \qquad v_{ab} = \left[v_{AB} - V_{AB}\right]$$

ending up with $i_d = g_d v_{ab}$

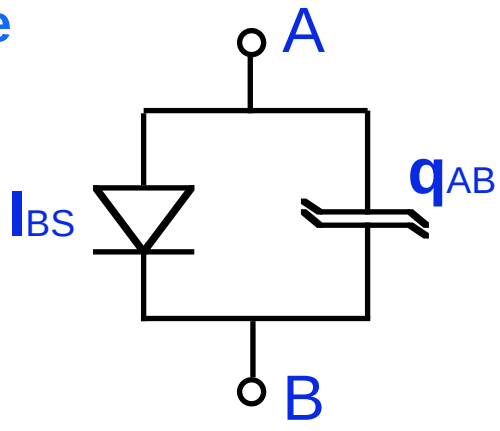


The corresponding LEC is shown at right:

LEC for p-n diodes (high f):

At high frequencies we must include the charge store, q_{AB}, and linearize its two components*:

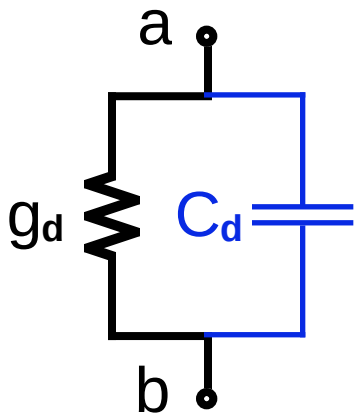
$$q_{AB} = q_{DP} + q_{QNR,p-side}$$



Depletion layer charge store, q_{DP}, and its linear equivalent capacitance, C_{dp}:

$$q_{DP}(v_{AB}) = -AqN_{Ap}x_p(v_{AB}) \approx -A\sqrt{2q\varepsilon_{Si}N_{Ap}(\phi_b - v_{AB})}$$

$$C_{dp}(V_{AB}) \equiv \left.\frac{\partial q_{DP}}{\partial v_{AB}}\right|_Q = A\sqrt{\frac{q\varepsilon_{Si}N_{Ap}}{2(\phi_b - V_{AB})}}$$



Diffusion charge store, $q_{QNR,p\text{-}side}$, and its linear equivalent capacitance, C_{df}:

$$q_{QNR,p-side}(v_{AB}) = \frac{i_D\left[w_p - x_p\right]^2}{2D_e}$$

$$C_{df}(V_{AB}) \equiv \left.\frac{\partial q_{QNR,p-side}}{\partial v_{AB}}\right|_Q = \frac{qI_D}{kT}\frac{\left[w_p - x_p\right]^2}{2D_e} = g_d\tau_d \quad \text{with} \quad \tau_d \equiv \frac{\left[w_p - x_p\right]^2}{2D_e}$$

* This discusion assumes an n^+-p diode)

Linear equivalent circuit for BJTs in FAR (low f):

In the forward active region, our static model says:

$$i_B(v_{BE},v_{CE}) = I_{BS}\left[e^{qv_{BE}/kT}-1\right]$$

$$i_C(v_{BE},v_{CE}) = \beta_o\left[1+\lambda v_{CE}\right] i_B(v_{BE},v_{CE}) = \beta_o I_{BS}\left[e^{qv_{BE}/kT}-1\right]\left[1+\lambda v_{CE}\right]$$

We begin by linearizing i_C about Q:

$$i_c(v_{be},v_{ce}) = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q v_{be} + \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q v_{ce} = g_m v_{be} + g_o v_{ce}$$

We introduced the transconductance, g_m, and the output conductance, g_o, defined as:

$$g_m \equiv \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q \qquad g_o \equiv \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q$$

Evaluating these partial derivatives using our expression for i_C, we find:

$$g_m = \frac{q}{kT}\beta_o I_{BS} e^{qV_{BE}/kT}\left[1+\lambda V_{CE}\right] \approx \frac{qI_C}{kT}$$

$$g_o = \beta_o I_{BS}\left[e^{qV_{BE}/kT}+1\right]\lambda \approx \lambda I_C \quad \left(\text{or} \approx \frac{I_C}{V_A}\right)$$

LEC for BJTs (low f), cont.:

Turning next to i_B, we note it only depends on v_{BE} so we have:

$$i_b(v_{be}) = \left.\frac{\partial i_B}{\partial v_{BE}}\right|_Q v_{be} = g_\pi v_{be}$$

The input conductance, g_π, is defined as:

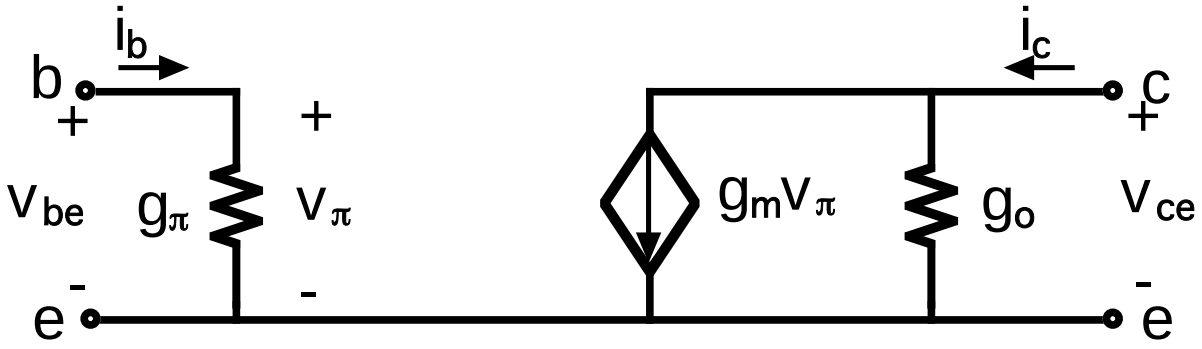
$$g_\pi \equiv \left.\frac{\partial i_B}{\partial v_{BE}}\right|_Q$$

(Notice that we do not define g_π as qI_B/kT)

To evaluate g_π we do not use our expression for i_B, but instead use $i_B = i_C/\beta_o$:

$$g_\pi \equiv \left.\frac{\partial i_B}{\partial v_{BE}}\right|_Q = \frac{1}{\beta_o}\left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q = \frac{g_m}{\beta_o} = \frac{qI_C}{kT\beta_o}$$

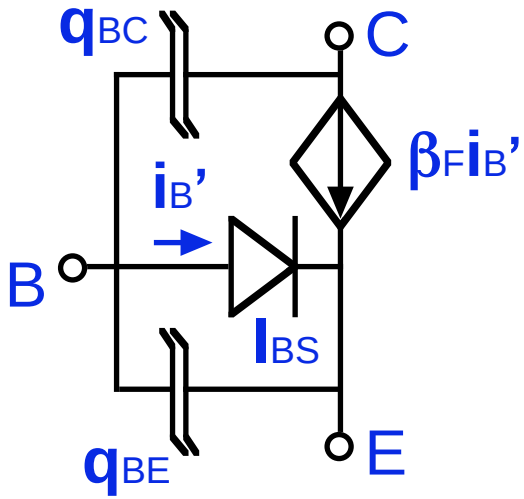
Representing this as a circuit we have:



(Notice that v_{be} is also called v_π)

LEC for BJTs (high f):

To extend the model to high frequency we linearize the charge stores associated with the junctions and add them.



The base-collector junction is reverse biased so the charge associated with it, q_{BC}, is the depletion region charge. The corresponding capacitance is labeled C_μ.

$$q_{BC}(v_{BC}) \approx -A\sqrt{2q\varepsilon_{Si}\left[\phi_{b,BC} - v_{BC}\right]N_{DC}} \qquad C_\mu(V_{BC}) \equiv \left.\frac{\partial q_{BC}}{\partial v_{BC}}\right|_Q = A\sqrt{\frac{q\varepsilon_{Si}N_{DC}}{2\left[\phi_b - V_{BC}\right]}}$$

The base-emitter junction is forward biased and its dominant charge store is the excess charge injected into the base; the base-emitter depletion charge store less important.

$$q_{BE}(v_{BE}) \approx Aqn_i^2 \frac{D_e}{N_{AB}w_{B,eff}}\left[e^{qV_{BE}/kT} - 1\right] \approx \frac{w_{B,eff}^2}{2D_e}\, i_C(v_{BE})$$

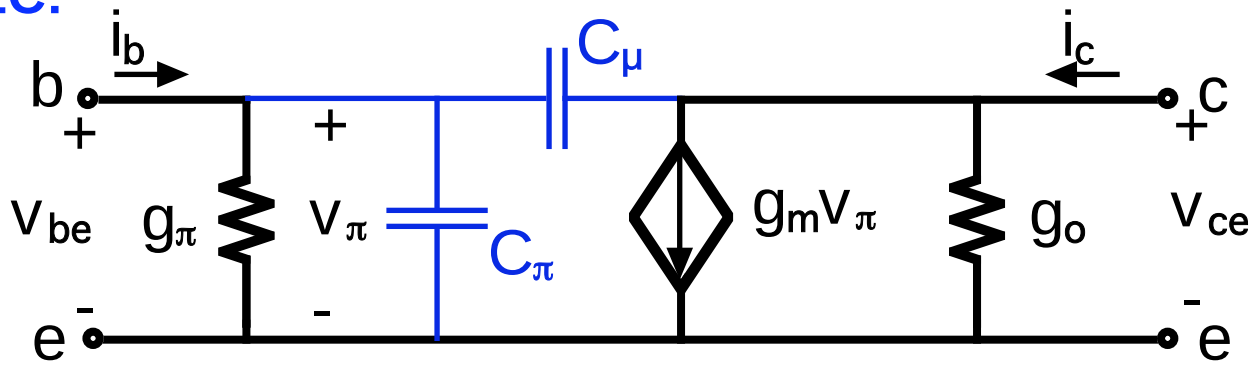
The linear equivalent capacitance is labeled C_π.

LEC for BJTs (high f), cont:

C_π can be written in terms of g_m and τ_b:

$$C_\pi(V_{BE}) \equiv \left.\frac{\partial q_{BE}}{\partial v_{BE}}\right|_Q \approx \frac{w_{B,eff}^2}{2D_e}\frac{qI_C}{kT} = g_m\tau_b \qquad \tau_b \equiv \frac{w_{B,eff}^2}{2D_e}$$

Adding C_π and C_μ to our BJT low frequency LEC we get the full BJT LEC:



$$g_m = \frac{qI_C}{kT} \qquad C_\mu = A\sqrt{\frac{q\varepsilon_{Si}N_{DC}}{2[\phi_b - V_{BC}]}}$$

$$g_\pi = \frac{g_m}{\beta_F} \qquad C_\pi = g_m\tau_b$$

$$g_o = \lambda I_C \quad (= I_C/V_A)$$

LEC for MOSFETs in saturation (low f):

In saturation, our static model is: (Recall that $\alpha \approx 1$)

$$i_G(v_{GS},v_{DS},v_{BS}) = 0 \qquad i_B(v_{GS},v_{DS},v_{BS}) \approx 0$$

$$i_D(v_{GS},v_{DS},v_{BS}) = \frac{K}{2\alpha}\left[v_{GS} - V_T(v_{BS})\right]^2\left[1+\lambda\left(v_{DS} - V_{DS,sat}\right)\right]$$

$$\text{with} \quad K \equiv \frac{W}{L}\mu_e C_{ox}^* \quad \text{and} \quad V_T = V_{To} + \gamma\left(\sqrt{\left|2\phi_{p-Si}\right| - v_{BS}} - \sqrt{\left|2\phi_{p-Si}\right|}\right)$$

Note that because i_G and i_B are zero they are already linear, and we can focus on i_D. Linearizing i_D about Q we have:

$$i_d(v_{gs},v_{ds},v_{bs}) = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q v_{ds} + \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q v_{bs}$$

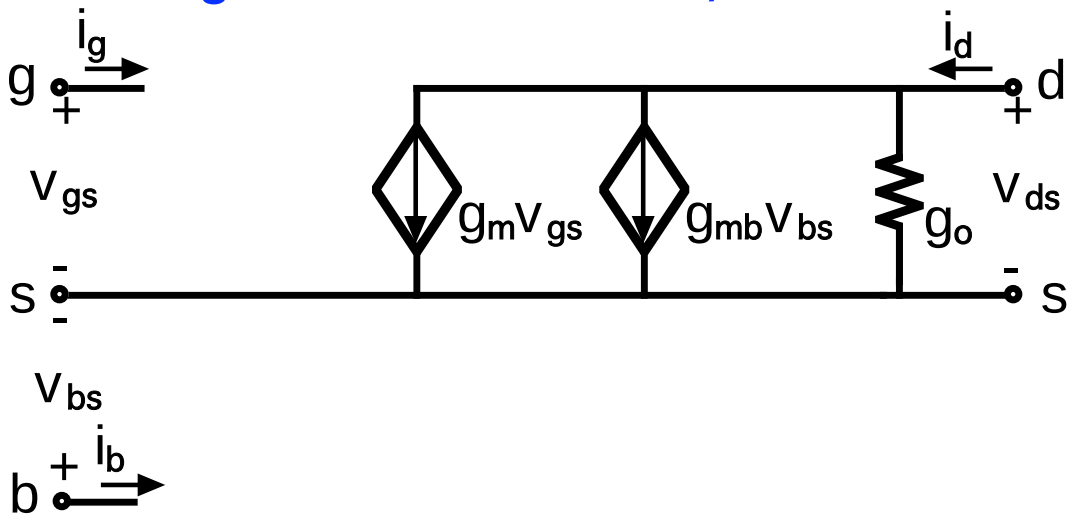
$$= g_m v_{gs} + g_o v_{ds} + g_{mb} v_{bs}$$

We have introduced the transconductance, g_m, output conductance, g_o, and substrate transconductance, g_{mb}:

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q \qquad g_o \equiv \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q \qquad g_{mb} \equiv \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q$$

LEC for MOSFETs in saturation (low f), cont.:

A circuit containing all these elements, i.e. the actual LEC, is:



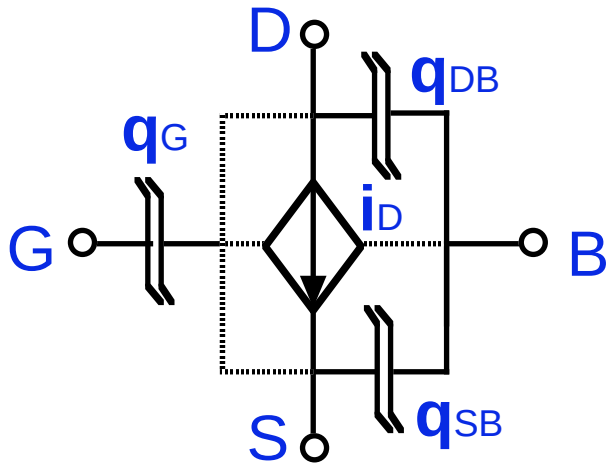
Evaluating the conductances in saturation we find:

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = \frac{K}{\alpha}\left[V_{GS} - V_T(V_{BS})\right]\left[1 + \lambda V_{DS}\right] \approx \sqrt{2K I_D/\alpha}$$

$$g_o \equiv \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = \frac{K}{2\alpha}\left[V_{GS} - V_T(V_{BS})\right]^2 \lambda \approx \lambda I_D$$

$$g_{mb} \equiv \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = -\frac{K}{\alpha}\left[V_{GS} - V_T(V_{BS})\right]\left[1 + \lambda V_{DS}\right]\left.\frac{\partial V_T}{\partial v_{BS}}\right|_Q = \eta g_m$$

LEC for MOSFETs in saturation (high f):



For the high frequency model we linearize and add the charge stores associated with each pair of terminals.

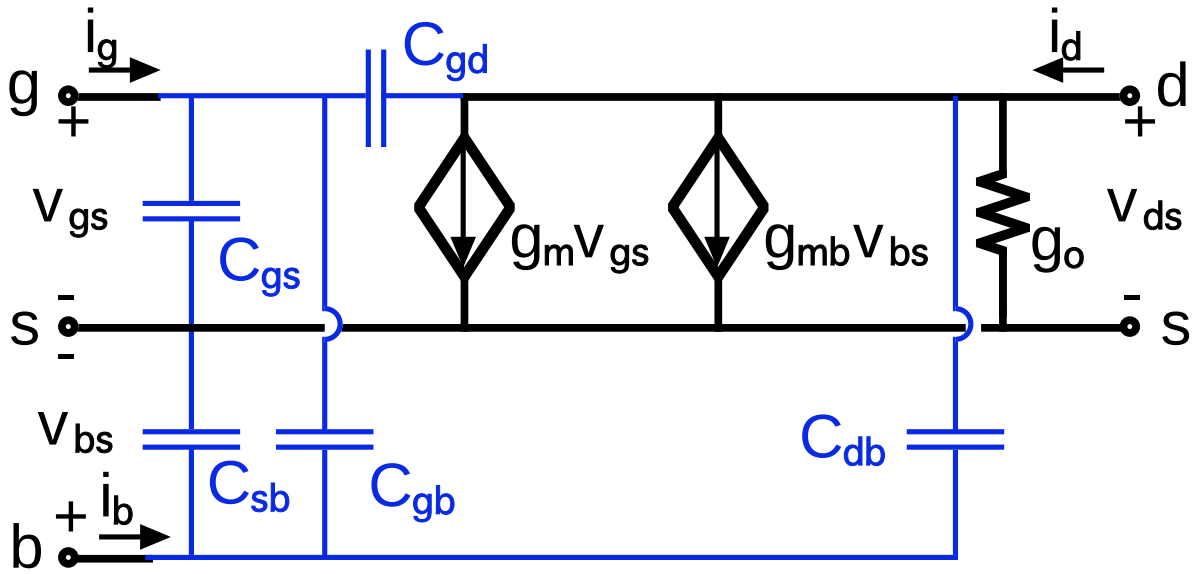
Two, q_{SB} and q_{DB}, are depletion region charge stores associated with the n+ regions of the source and drain. They are relatively straightforward compared to q_G., as we will see below. q_{SB} and q_{DB} contribute two capacitors, C_{sb} and C_{db}, to our LEC.

The gate charge, q_G, depends in general on v_{GS}, v_{DS}, and v_{GB} (= v_{GS}-v_{BS}), but in saturation, q_G only depends on v_{GS} and v_{GB} (i.e. v_{GS} and v_{BS}) in our model, adding C_{gs} and C_{gb}.

When $v_{GS} \geq V_T$ the drain is ideally decoupled from the gate , but in any real device there is fringing capacitance between the gate electrode and the drain diffusion that we must include as C_{gd}, a parasitic element.

LEC for MOSFETs in saturation (high f), cont.:

Adding all these capacitors to our LEC yields:



We find the following results:

$$C_{gs} \equiv \left.\frac{\partial q_G}{\partial v_{GS}}\right|_Q = \frac{2}{3} W L C_{ox}^*$$

$C_{gd} = W C_{gd}^*$, where C_{gd}^* is the G-D fringing and overlap capacitance per unit gate length (parasitic)

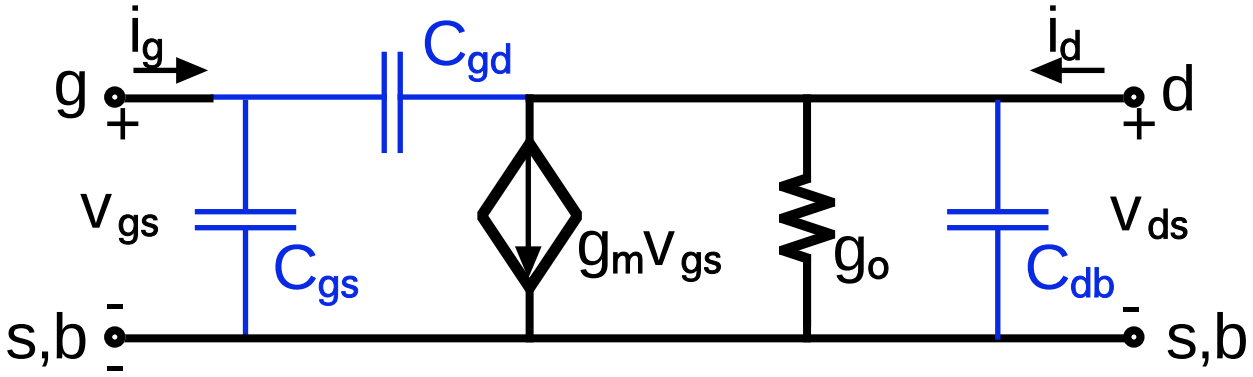
C_{sb}, C_{gb}, C_{db} : depletion capacitances

$$g_m \approx \sqrt{2K I_D/\alpha} \qquad g_o \approx \lambda I_D \qquad g_{mb} = \eta g_m, \text{ where } \eta = \gamma \Big/ 2\sqrt{|2\phi_p| - V_{BS}}$$

LEC for MOSFETs in saturation when $v_{bs} = 0$:

A very common situation in many circuits is that there is no signal applied between on the base, i.e. $v_{bs} = 0$ (even though it may be biased relative to the source, $V_{BS} \neq 0$).

In this case the MOSFET LEC simplifies significantly:



The elements that remain retain their original dependences:

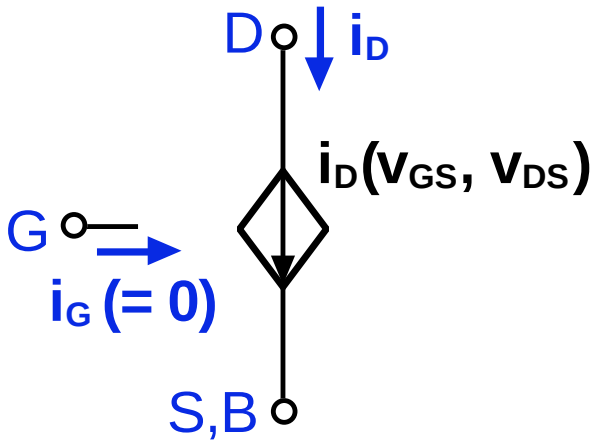
$$g_m \approx \sqrt{2K I_D/\alpha} \qquad g_o \approx \lambda I_D$$

$$C_{gs} \equiv \left.\frac{\partial q_G}{\partial v_{GS}}\right|_Q = \frac{2}{3} W L C_{ox}^* \qquad C_{gd} = W C_{gd}^*,$$ where C_{gd}^* is the G-D fringing and overlap capacitance per unit gate length (parasitic)

C_{db} : depletion capacitance

LEC for Sub-threshold MOSFETs, $v_{BS} = 0$:

Our large signal model for MOSFETs operated in the sub-threshold FAR ($v_{DS} >> kT/q$) and $v_{BS} = 0$, is:



$$i_{G,s-t}(v_{GS}, v_{DS}, v_{BS}) = 0$$

$$i_{D,s-t}(v_{GS}, v_{DS}) \approx I_{S,s-t}\left(1 - \lambda v_{DS}\right) e^{\{v_{GS} - V_{To}\}/nV_t}$$

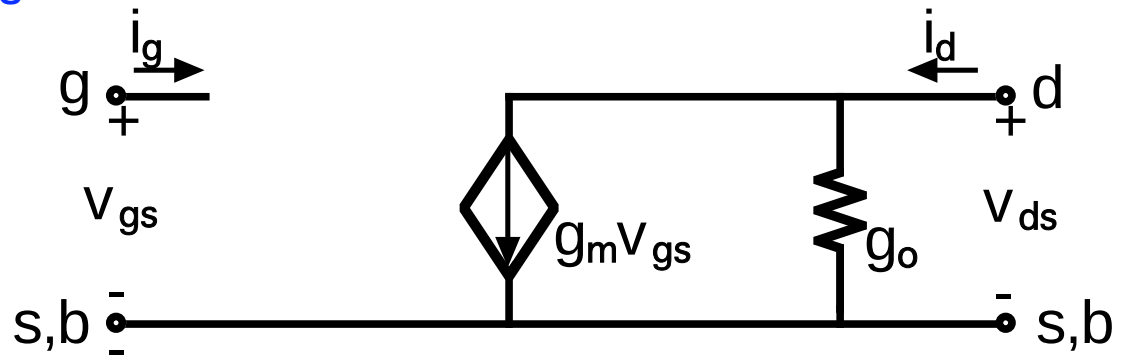
Like a MOSFET in saturation with $v_{bs} = 0$, the LEC has only two elements, g_m and g_o, but now g_m is quite different:

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = \frac{q}{nkT} I_{S,s-t}\left(1 - \lambda V_{DS}\right) e^{q(V_{GS} - V_{to})/nkT} = \frac{q I_D}{nkT}$$

$$g_o \equiv \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = \lambda I_{S,s-t}\, e^{q(V_{GS} - V_{to})/nkT} \approx \lambda I_D \quad \left(\text{or} \approx \frac{I_D}{V_A}\right)$$

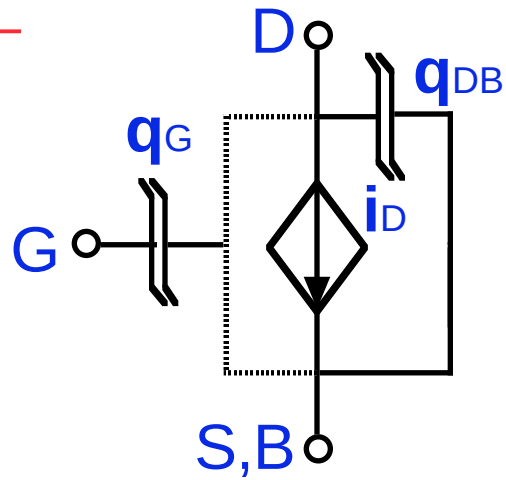
LEC for Sub-threshold MOSFETs, v_{BS} = 0, cont.:

The LEC for MOSFETs in sub-threshold FAR (v_{DS} >> kT/q) and v_{BS} = 0, is:



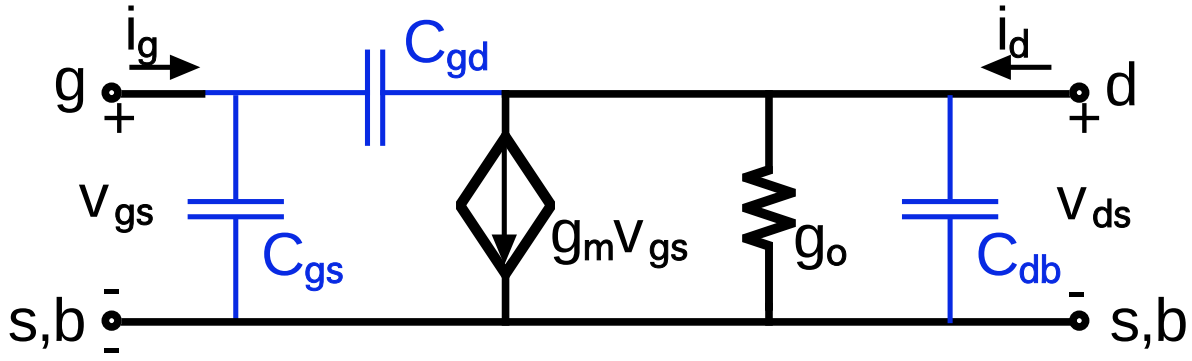
$$g_m = \frac{qI_D}{nkT} \qquad g_o \approx \lambda I_D$$

The charge store q_{DB} is the same as q_{DB} in a MOSFETs operated in strong inversion, but g_G is not. g_G is the gate capacitance in depletion ($V_{FB} < v_{GB} < V_T$), so it is smaller in sub-threshold.



LEC for Sub-threshold MOSFETs, v_{BS} = 0, cont.:

Adding the linear capacitors corresponding to the charge stores we have:



$$C_{gs} \equiv \left.\frac{\partial q_G}{\partial v_{GS}}\right|_Q = W\,L\,C_{ox}^{*} \Big/ \sqrt{1+\frac{2C_{ox}^{*2}\left(V_{GS}-V_{FB}\right)}{\varepsilon_{Si} q N_A}}$$

*** See Lecture 9, Slides 7 and 8, for q_G and the derivation of C_{gs}.**

$C_{gd} = W\,C_{gd}^{*}$, where C_{gd}^{*} is the G-D fringing and overlap

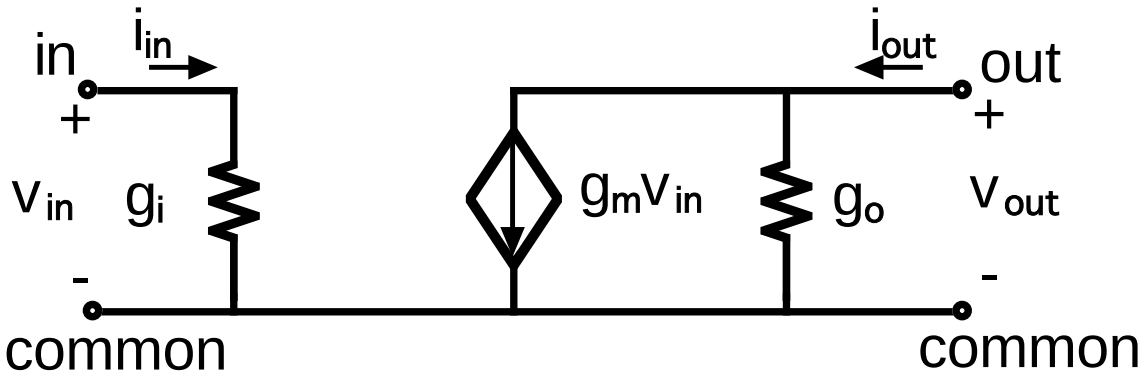
C_{db} : depletion capacitance

$$g_m = \frac{qI_D}{nkT} \qquad g_o \approx \lambda I_D$$

Notice that as before, C_{gd} is zero in our ideal model. It a parasitic that cannot be avoided and must be included because it limits device and circuit performance.

Comparing the low frequency LECs:

All of our circuit design will be done for operation at "low" frequencies, that is where the charge store capacitances play a negligible role. Thus it is interesting to compare our three transistor LECs when this is true. They all have the same topology, but differ importantly in g_i and g_m:



Bias dependences:

	BJT	ST MOS	SI MOS
g_i :	$qI_C/\beta_F kT$	0	0
g_m :	qI_C/kT	qI_D/nkT	$\sqrt{2KI_D/\alpha}$
g_o :	λI_C	λI_D	λI_D

ST = sub-threshold
SI = strong inversion

*** We will say more about the significance of these differences when we study amplifier design.**

The importance of the bias current:

A very important observation is that all of the elements in the three LECs we compared depend on the bias level of the output current, I_C, in the case of a BJT, or I_D, in the case of a MOSFET:

Bias dependences:

	BJT	ST MOS	SI MOS
g_i :	$qI_C/\beta_F kT$	0	0
g_m :	qI_C/kT	$qI_D/n\,kT$	$\sqrt{2KI_D/\alpha}$
g_o :	λI_C	λI_D	λI_D

ST = sub-threshold
SI = strong inversion

The bias circuitry is a key part of any linear amplifier. The designer must establish a stable bias point for all the transistors in the amplifier to insure that the gain remains constant and stable.

We will study amplifier design and practice beginning with Lecture 17.

Lecture 13 - Linear Equivalent Circuits - Summary

- **Reminder**
  - **Exam Two -** In ~1 wk., Thursday, Nov. 5, 7:30-9:30 p.m.
  - **Sub-Threshold Refs -** Lecture 12 slides; Sub-threshold write-up
- **Notation**
  - **Total = Bias + Signal**

$$i_A(t) = I_A + i_a(t)$$
$$v_{AB}(t) = V_{AB} + v_{ab}(t)$$

  - **Large signal model -** Design and analysis of bias conditions
  - **Linear equivalent circuits -** Signal portion design/analysis
- **Small signal models; linear equivalent circuits**
  - **Everything depends on the bias point -** The value of each element in an LEC depends on the bias point (often the bias current).
  - **Concentrate for now on low frequency LECs -** Full spectrum LECs with capacitors will only be used to find the upper bound on the low frequency range of operation. We won't see them again until Lecture 23.

6.012 Microelectronic Devices and Circuits

Fall 2009