*YOUR NAME*_____

*Department of Electrical Engineering and Computer Science*
*Massachusetts Institute of Technology*

# *6.012 Electronic Devices and Circuits*

## Exam No. 2

**Thursday, November 5, 2009**

**7:30 to 9:30 pm**

**Notes:**

1. An effort has been made to make the various parts of these problems independent of each other so if you have difficulty with one item go on, and come back later.
2. Some questions ask for an explanation of your answer. No credit will be given for answers lacking this explanation.
3. Unless otherwise indicated, you should assume room temperature and that kT/q is 0.025 V. You should also approximate [(kT/q) ln 10] as 0.06 V.
4. Closed book; one sheet (2 pages) of notes permitted. Formula sheet provided.
5. The best way to receive partial credit is to show your work. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
6. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
7. Be careful to include the correct units with your answers when appropriate.
8. Be certain that you have all ten (10) pages of this exam booklet and the six (6) page formula sheet, and make certain that you write your name at the top of this page in the space provided.

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|---|---|---|---|
| 6.012 Staff Use Only | **PROBLEM 1** | _____ | (out of a possible 32) |
| | **PROBLEM 2** | _____ | (out of a possible 34) |
| | **PROBLEM 3** | _____ | (out of a possible 34) |
| | **TOTAL** | | |

**Problem 1 -** (32 points)

This problem contains 3 independent short problems that can be worked in any order.

a) [8 pts] Consider an n-channel MOSFET with a channel length, L = 0.2 $\mu$m; width, W = of 5.0 $\mu$m; electron mobility, $\mu_e$ = 600 $cm^2/V\text{-}s$; and gate oxide capacitance, $C^*_{ox}$ = $10^{-8}\ F/cm^2$. The flatband voltage, $V_{FB}$ = - 0.2 V, and the threshold voltage, $V_T$ = +0.5 V. The bias voltages are $V_{BS} = V_{DS} = 0$ V.

i) The MOSFET is initially biased at flatband, and then at t = 0, $v_{GS}$ is changed from $V_{FB}$ to $V_{FB}$ - 1 V. After any transient, what is the total amount of any additional mobile charge at the oxide-semiconductor interface, and is it holes or electrons?

Electrons _____ Holes _____ Total amount of charge: _____ Coul

ii) Where do the additional carriers in Part (a-i) come from?

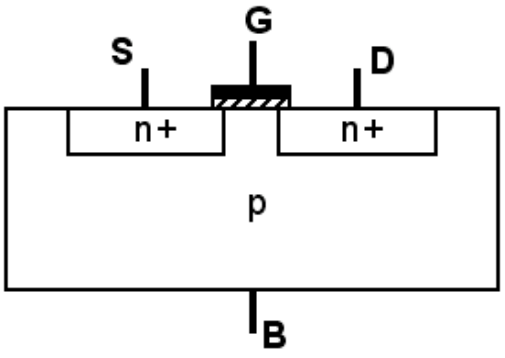
iii) The MOSFET is initially biased at threshold, and then at t = 0, $v_{GS}$ is changed from $V_T$ to $V_T$ + 1 V. After any transient, what is the total amount of any additional mobile charge at the oxide-semiconductor interface, and is it holes or electrons?

Electrons _____ Holes _____ Total amount of charge: _____ Coul

iv) Where do the additional carriers in Part (a-iii) come from?

b) [10 pts] Consider operating the enhancement-mode n-channel MOSFET shown to the right as a lateral npn bipolar transistor. Leave the gate disconnected and focus on terminals B, S, and D.

i) Label the terminals B, S, and D in the figure with their corresponding BJT roles (E, emitter; B, base; and C, collector), and specify the approximate voltage levels and polarities needed to bias the BJT in the forward active region.




$V_{CE}$: _____

$V_{BE}$: _____

**Problem 1 continues on the next page**

**Problem 1 continued**

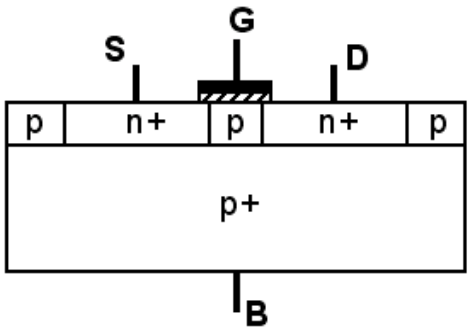
ii) If you measured the forward current gain, $\beta_f$, of this BJT, you would find that it is small, perhaps even less than 1, and if you measured the Early voltage, $V_A$, you would find it is relatively low. Explain each of these observations:

The forward current gain, $\beta_f$, is small because

The Early voltage, $V_A$, is low because

iii) Fabricating a lateral BJT with an underlying p+ layer as shown to the right improves one of the two parameters identified in Part (b-ii), but has little impact on the other. Which is parameter is improved and why?

_____ because




c) [14 pts] Graphene, a single atomic layer of carbon atoms, can be n- or p-type and its hole and electron mobilities are both 100,000 $cm^2/V\text{-}s$. Such excellent mobilities have led people to study using graphene-based FETs in high performance digital and/or analog electronics. The characteristics of one such FET are given by the expressions:

$$i_G(v_{GS},v_{DS}) = 0, \qquad i_D(v_{GS},v_{DS}) = \frac{W}{L}\mu\left[C^*_{ox}v_{GS} + \alpha\right]v_{DS} \quad \text{for} \quad v_{GS} \geq 0,\ v_{DS} \geq 0$$

where W and L are the gate width and length, respectively, $\mu$ is the carrier mobility, $C^*_{ox}$ is the oxide capacitance per unit area, and $\alpha$ accounts for the current at $v_{GS} = 0$ V.

i) Calculate an expression for the small-signal drain-to-source current, $i_{ds}$, in a graphene transistor, as a linear function of the small-signal gate-to-source voltage and drain-to-source voltages, $v_{gs}$ and $v_{ds}$, respectively, valid about the bias point, $V_{GS}$, $V_{DS}$.

$i_{ds}$ = _____

**Problem 1 continues on the next page**

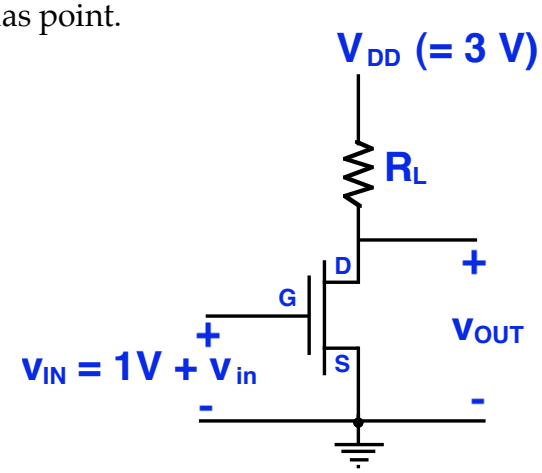
**Problem 1 continued**

ii) In the space provided below, draw a small signal linear equivalent circuit for the graphene transistor for a bias point ($V_{GS}$, $V_{DS}$), and give expressions for each of the elements in the circuit in terms of device and bias parameters.

iii) The output characteristics of graphene transistors recently fabricated at MIT can be fit by the expression:

$$i_D = 1 \times 10^{-7} (10\, v_{GS} + 1)\, v_{DS}$$

Where the voltages are in measured in Volts, and the current is Amps. Consider using this device in the amplifier illustrated below with $V_{DD}$ = 3 V and with the gate biased at 1 V. Select $R_L$ to give a DC output voltage of 1.5 V, and calculate the small signal voltage gain, $v_{out}/v_{in}$. at this bias point.



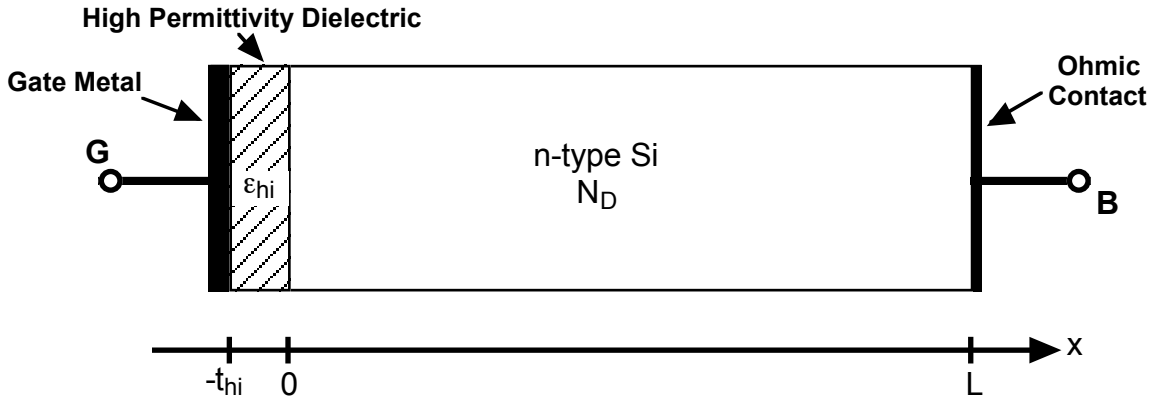

$R_L$ = _____ Ohms

$A_v = v_{out}/v_{in}$ = _____

**End of Problem 1**

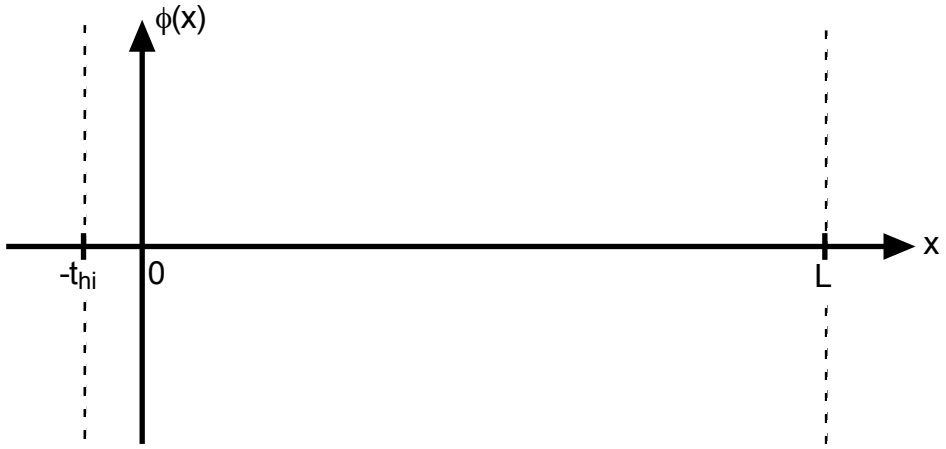
**Problem 2 -** (34 points)

Alice is a process engineer experimenting with a new high-permittivity dielectric material with a dielectric constant, $\varepsilon_{hi}$, that is 5 times as large as the dielectric constant of $SiO_2$.: $\varepsilon_{hi} = 5\,\varepsilon_{ox}$ She chooses to test the material by fabricating p-MOS capacitors on n-type silicon, and to use a metal for the gate and contact for which $\phi_m = -0.5\,\phi_n$. Her structure is illustrated below; it also includes an adjacent p+ region shorted to the substrate (not shown in the figure) to supply holes when an inversion layer is formed.




**Warning**: This is a p-MOS problem (i.e. p-channel); n-MOS answers will not be accepted.

a) [6 pts] On the axes provided, plot the electrostatic potential, $\phi(x)$, through the device from G to B (i.e. starting in the gate metal and going into the ohmic contact metal) in <u>flatband</u> when $v_{GB} = V_{FB}$. Label all relevant features on your plot, including values for $\phi(0)$, depletion region width, and potential drop across the oxide. Finally, derive an expression for the flatband voltage, $V_{FB}$.




$V_{FB}$ = _____

**Problem 2 continues on the next page**

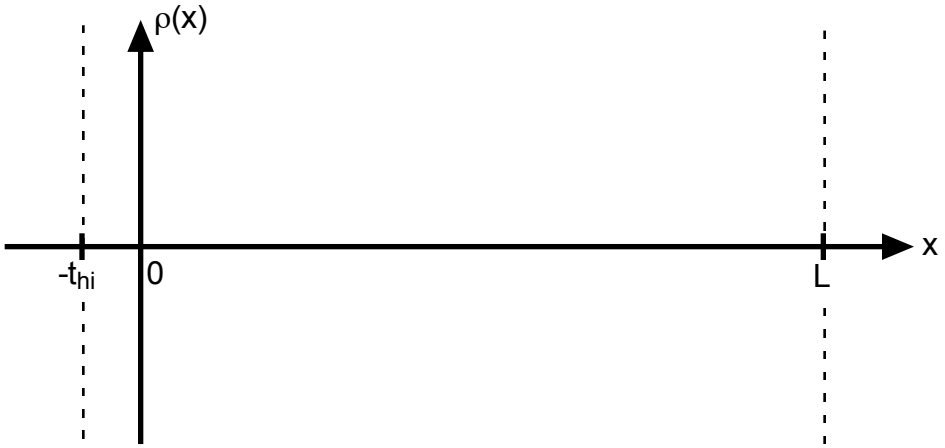
**Problem 2 continued**

b) [4 pts] At flatband, i.e. with $v_{GB} = V_{FB}$, what are the electron and hole concentrations, $n(x = 0^+)$ and $p(x = 0^+)$, at the silicon-dielectric interface?

$n(x = 0^+) =$_____

$p(x = 0^+) =$_____

c) [8 pts] On the axes provided, plot the electrostatic potential, $\phi(x)$, and the charge distribution, $\rho(x)$, through the device from G to B at the onset of inversion, i.e. when $v_{GB} = V_T$. Label all relevant features on your plots, including values for $\phi(0)$, depletion region width, and potential drop across the oxide. Finally, derive an expression for the threshold voltage, $V_T$.


$V_T =$_____

**Problem 2 continues on the next page**

**Problem 2 continued**

d) [4 pts] At the onset of inversion, i.e., when $v_{GB} = V_T$,what are the electron and hole concentrations, $n(x = 0^+)$ and $p(x = 0^+)$, at the silicon-dielectric interface?

$n(x = 0^+) =$_____

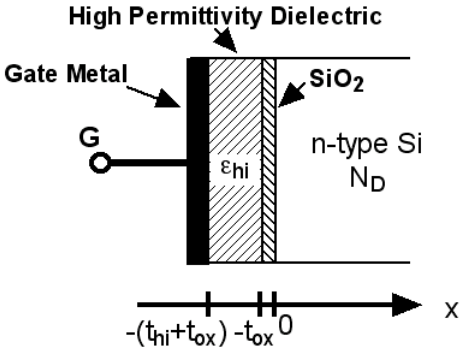
$p(x = 0^+) =$_____

e) [8 pts] A practical problem with depositing a dielectric other than $SiO_2$ directly on silicon is that new energy states and/or fixed sheet charge are introduced at the interface. Imagine that the latter occurs, and that there is a fixed positive sheet charge density, $\sigma_i$, at the interface. Assuming that this charge can be modeled as an impulse of charge of intensity $\sigma_i$ at $x = 0$, i.e. $\rho(x) = \sigma_i \delta(x)$, calculate the changes in the flatband voltage, $V_{FB}$, and in the threshold voltage, $V_T$, resulting from the presence of this charge.

Flatband voltage, $\Delta V_{FB}$: _____

Threshold voltage, $\Delta V_T$: _____

f) [4 pts] To eliminate the interface charge, a very thin layer of silicon dioxide, $SiO_2$, can be grown on the silicon before the high permittivity dielectric is deposited, as illustrated to the right. How much is the gate dielectric capacitance, $C_G$, changed relative to its original value in Part (a) by the addition this $SiO_2$ layer if $t_{ox} = 0.2\ t_{Hi}$?




$C_G(\text{w. } SiO_2)/C_G(\text{w.o. } SiO_2) =$ _____

**End of Problem 2**

**Problem 3 -** (34 points)

This problem studies the performance of state-of-the-art MOSFET transistors in digital electronics. In modern CMOS technology, the physical parameters of transistors with minimum dimensions are as follow:

| | |
|---|---|
| Gate oxide thickness, $t_{ox}$: | 1.0 nm ($10^{-7}$ cm) |
| Oxide dielectric constant, $\varepsilon_{ox}$: | $3.5 \times 10^{-13}$ F/cm |
| Gate length, $L_{min}$: | 35 nm |
| Gate width, $W_{min}$: | 135 nm |
| Supply voltage, $V_{DD}$: | 1.0 V |
| Threshold voltage: | $V_{T,n} = -V_{T,p} = 0.4$ V |
| Electron mobility, $\mu_e$: | 500 $cm^2/Vs$ |
| Hole mobility, $\mu_h$: | 200 $cm^2/Vs$ |
| Sub-threshold current when $\lvert V_{GS} \rvert = 0$: | 15 nA (n-channel and p-channel) |
| Early effect: | $\lambda_n = \lambda_p = 10^{-3}\ V^{-1}$ |
| Alpha factor, $\alpha$: | $\approx 1$ |

a) [5 pts] Calculate the drain current in saturation, $I_{D,sat}$, of a minimum size n-MOS transistor in this technology when $V_{GS} = V_{DS} = V_{DD} = 1.0$ V. Use the general expression we derived using the gradual channel approximation model in strong inversion and assume $\alpha = 1$ and that the low-field mobility model is valid.

$I_{D,sat}(V_{GS} = V_{DS} = 1.0\ V) =$ _____ A

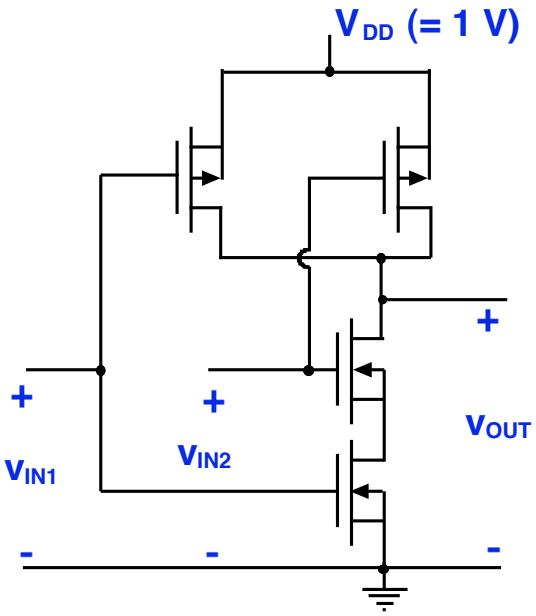
b) [5 pts] Calculate the value of the output resistance, $r_o$, in the small signal linear equivalent circuit of the n-MOS transistor in saturation with $V_{GS} = 1.0$ V. [If you could not do Part a use a drain current of 1 mA (this is not the right answer for Part a).]

$r_o =$ _____ Ohms

**Problem 3 continues on the next page**

**Problem 3 continued**

The CMOS NAND gate shown to the right is fabricated using the new technology.




c) [4 pts] Fill in the truth table below for this gate. Ignore the sub-threshold drain current when the FETs are off.

| $V_{IN1}$ | $V_{IN2}$ | $V_{OUT}$ |
|---|---|---|
| 0 V | 0 V | _____V |
| 0 V | 1 V | _____V |
| 1 V | 0 V | _____V |
| 1 V | 1 V | _____V |

d) [4 pts] In a simple CMOS inverter both transistors are minimum gate length devices, $L_n = L_p = L_{min}$, and the widths are scaled so that $K_n = K_p$, with the narrowest gate being made $W_{min}$. What should $W_n$ and $W_p$ be in a simple inverter made with this process (i.e., as described at the start of this problem statement)? Note: The multiples do not have to be integer.

$W_{n,Inverter}$ = _____ $W_{min}$

$W_{p,Inverter}$ = _____ $W_{min}$

e) [4 pts] To size the FETs in a NAND gate for minimum switching time, one must recognize that two n-FETs in series with the same voltage on their gates, as in a NAND gate when both inputs are high, function like one FET with $L = 2L_n$ (and $W = W_n$). What is the optimum size of the n-channel MOSFETs in a NAND gate fabricated with the process described earlier, and what is the load seen at the input of such a NAND gate, compared to an inverter? Note: The multiples can be non-integer. (The p-channel FET should be kept the same size as in a simple inverter because turning either p-FET "on" pulls the output high.)

$L_{n,NAND}$ = _____ $L_{min}$

$W_{n,NAND}$ = _____ $W_{min}$

$C_{IN,NAND}$ = _____ $C_{IN,Inverter}$

**Problem 3 continues on the next page**

**Problem 3 continued**

f) [4 pts] What is the static power dissipation in a microprocessor containing $2 \times 10^9$ equivalent inverter gates? Assume that for half of the gates the output is low and for half of the gates it is high.

$P_{Static}$ = _____ Watts

g) [8 pts] When the n-channel transistor in Part a) was fabricated, the actual saturation current with $V_{GS} = V_{DS} = 1$ Volt was measured to be only 250 μA. To try to figure out what is wrong, do the following three calculations, and then give an opinion:

i) Calculate the average electric field in the channel with $V_{GS} = V_{DS} = 1$ Volt.

$E_{ave}$ = _____ V/cm

ii) Calculate what the average electron velocity in the channel with $V_{GS} = V_{DS} = 1$ Volt and a drain current of 250 $\mu$A is. Assume a uniform inversion charge distribution along the channel.

$s_{ch\ ave}$ ($I_D = 250\ \mu A$) = _____ cm/s

Calculate what the average electron velocity in the channel would be with $V_{GS} = V_{DS} = 1$ Volt and the drain current you calculated in Part a. Approximate the inversion charge distribution along the channel as being uniform. If you could not do Part a use a drain current of 1 mA (this is not the right answer for Part a).

$s_{ch,ave}$ ($I_D$ = answer in Part a) = _____ cm/s

iii) Why (in 25 words or less) do you think the measured drain current is so much lower than you predicted in Part a?

**End of Problem 3 and of Exam Two**

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