MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.012 MICROELECTRONIC DEVICES AND CIRCUITS

Problem Set No. 9

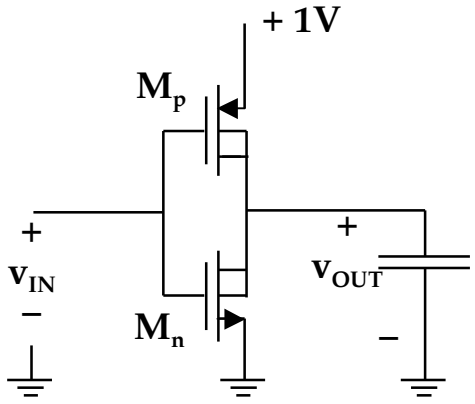
Issued: November 6, 2009 (corrected 11/9) **Due:** November 13, 2009

Reading Assignments:
Lecture 17 (11/10/09) - Chap. 11 (11.1, 11.2)
Lecture 18 (11/12/09) - Chap. 11 (11.4)
Lecture 19 (11/17/09) - Chap. 12 (12.1, 12.2, 12.3)

Problem 1 - The p- and n-channel MOSFETs in this question have the following parameter values:

$$(W_n/L_n)\mu_n C_{ox} = (W_p/L_p)\mu_p C_{ox} = 5 \times 10^{-4}\ A/V^2,\ V_{Tn} = 0.25\ V,\ V_{Tp} = -0.25\ V$$
$$g_{mb} = 0.2\ g_m,\ \lambda_n = \lambda_p = 0.05\ V^{-1},\ |V_{ON\text{-}substrate\ diodes}| = 0.7\ V$$

a) An n-channel MOSFET and p-channel MOSFET are connected to form a CMOS gate, but the substrate contacts are mistakenly connected to the drains of their respective transistors, as illustrated to the right. Your task in this question will be to determine the impact of this mistake on the transfer characteristic of this inverter.



i) Draw the low frequency small signal linear equivalent circuit for this inverter at the bias point $V_{IN} = V_{OUT} = V_M = V_{DD}/2$. Evaluate g_{mn}, g_{mp}, g_{mbn}, g_{mbp}, g_{on}, and g_{op}, and indicate which, if any, of these parameters have the same values.

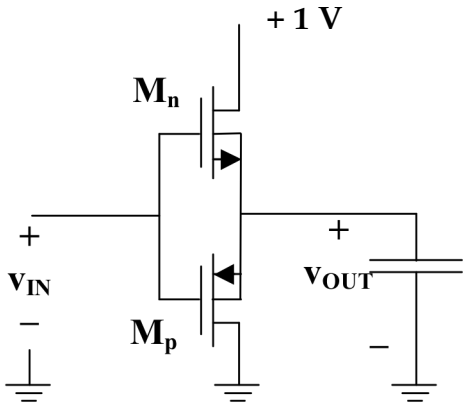
ii) What is the slope of the transfer function of this inverter at this bias point, i.e., $V_{IN} = V_{OUT} = V_M = V_{DD}/2$? Express your answer in terms of the g_{xx}'s and simplify it as much as you can. Then also express your answer in terms of the bias point voltages and currents. Compare your answer to that of the correct connection.

iii) Given that the substrate p-n junction diode turn on voltage is 0.7 V, sketch V_{out} vs V_{in} (the inverter transfer characteristic).

b) The engineer who made the layout mistake in Part (a) also made a layout mistake at his pervious job, and it was a rather more serious blunder (which is why he now has a different job). While trying to design a CMOS inverter he connected the n-MOS transistor to the + 1 V supply and the p-MOS transistor to ground, as shown in the figure on the next page.

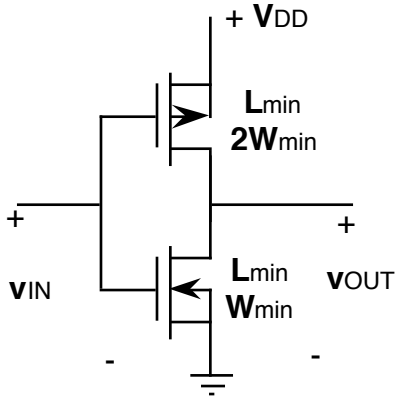
i) When v_{IN} has been 0 Volts for a long time, v_{OUT} is also 0 Volts. Starting at this point, consider increasing v_{IN} to 1 Volts. What is v_{OUT} when v_{IN} reaches 1 Volts? Make certain it is clear to the grader how you got your answer.

ii) After v_{IN} has been incresed to 1 Volts as in Part c)i) above, it is again reduced to 0 Volts. What is v_{OUT} when v_{IN} reaches 0 Volts now? HINT: It is not 0 Volts.



iii) Sketch v_{OUT} vs v_{IN} starting at the condition in Part c)ii) and increasing v_{IN} to 1 V, and then decreasing it back to 0 V.

Problem 2 - This problem deals with CMOS inverters fabricated using a process in which the minimum gate length and width are L_{min} and W_{min}, respectively. In order to obtain symmetrical transfer characteristics and minimize the gate delay, the inverters are designed to have $V_{Tn} = |V_{Tp}|$, $t_{oxn} = t_{oxp}$, and $K_n = K_p$. All the inverters have minimum length gates, i.e., $L_n = L_p = L_{min}$, and the width of the p-channel devices is twice that of the n-channel devices, i.e., $W_p = 2W_n$, because the hole and electron mobilities in the channel differ by a factor of two, i.e., $\mu_e = 2\,\mu_p$. The smallest inverters have $W_n = W_{min}$ and $W_p = 2\,W_{min}$, and we will call the corresponding K value K_{min}.



This minimum size inverter is shown above. The gate delay, τ_{GD}, of this minimum size inverter is found to be 100 ps (10^{-10} s) when the fan-out is one. We will call this gate delay the minimum gate delay, τ_{min}.

(a) What is the gate delay of a minimum-size inverter that has a fan-out of four, i.e., when its output is connected to four stages?

(b) The inverters which drive the bond pads and the wires going to other chips must supply much larger currents because they have much larger capacitances to charge and discharge than do the inverters which simply drive other inverters on the same chip. We will call these "output inverters." Suppose that on the present chip, the MOSFETs in the output inverters must have K values of 100 K_{min}.

(i) What are W_n and W_p of the devices in the output inverters?

(ii) What is the input capacitance of these output stages in terms of the input capacitance of a minimum-size inverter, which you can call C_{min}?

(iii) What would the gate delay be for a minimum-size inverter loaded with a single output inverter stage, i.e., loaded with the capacitance you found above in Part (c)(ii)?

(c) Consider inserting an inverter stage with K = 10 K_{min} between the minimum-size inverter and an output inverter.

(i) Draw the circuit schematic for these three inverter stages, indicating next to each device its gate width.

(ii) What are the gate delays, τ_{GD}'s, for the first (K_{min}) and second (10 K_{min}) stages in this circuit?

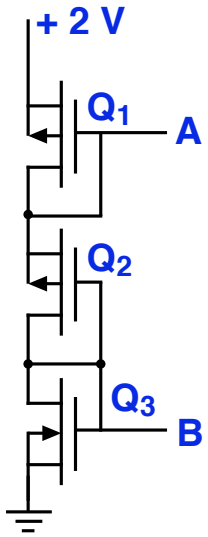
(iii) What is the total delay going through both the K_{min} and 10 K_{min} stages, and how does it compare with your answer in Part (c)(iii)?

(iv) If one intermediate stage before an output stage is good, are two better? How about n, where n > 2? Is there an optimum n?

Problem 3 - A couple of problems on current source bias design.

(a) Do Problem 12.6 in the course text.

(b) In integrated circuits, bias stack resistors like that in the circuit of the previous problem, are often replaced by MOSFETs with their gates connected to their drains. This is attractive because resistors consume a lot of space on a chip, and are hard to fabricate with precise values. An example is the circuit on the right. Use the transistor specifications at the end of this problem set to answer the following questions about this circuit.



a) Design the gate widths and lengths of Q_1, Q_2, and Q_3 so that V_A = 1.3 V and V_B = 0.7V. Keep the power dissipation as low as possible, and give its value.

b) Now design the gate widths and lengths of Q_1, Q_2, and Q_3 so that V_A = 1.2 V and V_B = 0.6V. Again keep the power dissipation as low as possible, and give its value.

Problem 4 - A two-part problem.

(a) Consider the common-source stage with shunt feedback shown on Foil 22 of Lecture 18.

(i) Use the linear equivalent circuit shown on the foil to calculate the input resistance of this stage.

(ii) Write your result from Part a in terms of the magnitude of the voltage gain of the stage. See if you can explain why R_F looks like a much smaller resistor than it really is. This is called the Miller Effect.

(b) The two-port voltage gain of a common-source amplifier is $-g_m/(g_o+g_{sl})$ as was discussed in Lecture 18 (see Foil 15); this is also true for the BJT version of this stage, which is called a common-emitter amplifier. The magnitude of this two-port voltage gain occurs when the stage load is infinite ($g_{sl} = 0$), and it is $A_{v,max} = g_m/g_o$.

Consider common-source/-emitter amplifiers made with the following transistors and for each find an expression for $A_{v,max}$ in terms of the quiescent drain current, I_D, and determine for each if there is a bias current that maximizes $A_{v,max}$, and what it is.

(i) An n-channel enhancement mode MOSFET biased in saturation (strong inversion) for which velocity saturation is not important.

(ii) An n-channel enhancement mode MOSFET biased in the sub-threshold region.

(iii) A very short gate n-channel enhancement mode MOSFET biased in saturation (strong inversion) in which velocity saturation dominates at even small drain-to-source voltages.

(iv) An npn BJT biased in its forward active region.

MOSFET Specifications for Problem 3: (there is more information here than you need)

1. n-channel MOSFET's -- The n-channel MOSFET's are enhancement-mode devices with the following large and small-signal parameters.
   - *a)* *Minimum size devices ($W = W_{min}$, $L = L_{min}$)*
     - i) $K = 2.0\ mA/V^2$ $\qquad \alpha = 1$
     - ii) $V_T = +0.5\ V$
     - iii) $g_m = K(V_{GS}-V_T) = (2KI_D)^{1/2} = 2I_D/(V_{GS}-V_T)$
       $g_o = \lambda I_D = I_D/|V_A|$ with $|V_A| = 5\ V$
     - iv) Operating range: $(V_{GS} - V_T) \geq 0.1\ V$
   - *b)* *Scaled devices* -- The width of the gate (and channel), W, can be as large as $100\ W_{min}$, and the length can be long as $2\ L_{min}$.
2. p-channel MOSFET's -- The p-channel MOSFET's are enhancement-mode devices with the following large and small-signal parameters.
   - *a)* *Minimum size devices ($W = W_{min}$, $L = L_{min}$)*
     - i) $K = 1.0\ mA/V^2$ $\qquad \alpha = 1$
     - ii) $V_T = -0.5\ V$
     - iii) $g_m = K(V_{SG}-|V_T|) = (2K|I_D|)^{1/2} = 2|I_D|/(V_{SG}-|V_T|)$
       $g_o = \lambda|I_D| = |I_D|/|V_A|$ with $|V_A| = 5\ V$
     - iv) Operating range: $(V_{SG} - |V_T|) \geq 0.1\ V$
   - *b)* *Scaled devices* -- The width of the gate (and channel), W, can be as large as $100\ W_{min}$, and the length can be as long as $2\ L_{min}$.

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