November 16, 2005 - Quiz #2

Name: SOLUTIONS

Recitation: _____

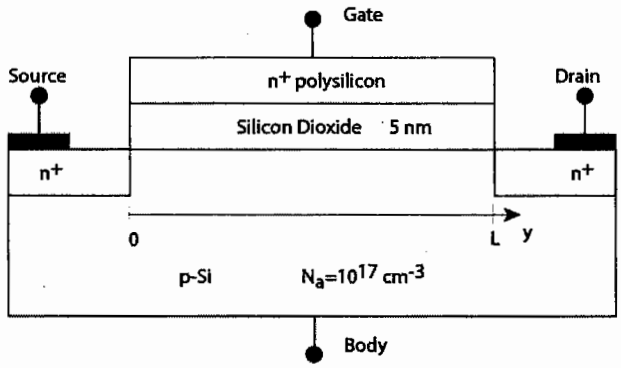
problem	grade
1	
2	
3	
4	
total	

General guidelines (please read carefully before starting):

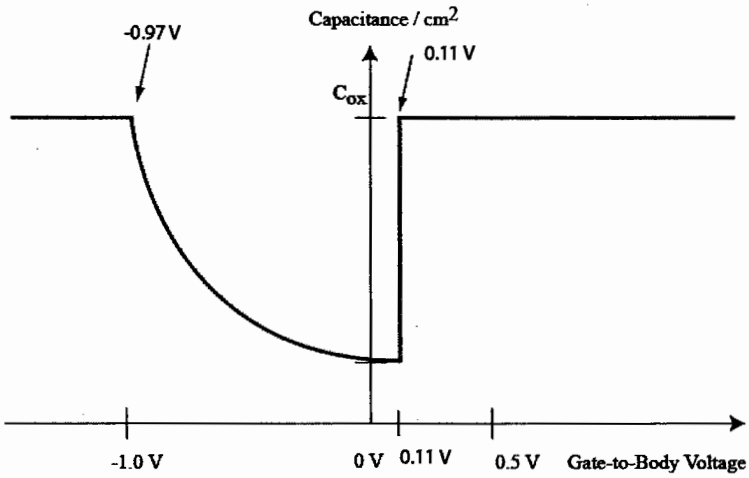
- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back of the page.
- You have **120 minutes** to complete your quiz.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, E, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use $\phi = 0$ at $n_o = p_o = n_i$ as potential reference.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$$n_i = 1 \times 10^{10}\ cm^{-3}$$
$$kT/q = 0.025\ V$$
$$q = 1.60 \times 10^{-19}\ C$$
$$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$$
$$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$$

1. *(30 points)* Below is an n^+ - polysilicon-gate MOSFET. The substrate doping is $N_a = 10^{17}\ cm^{-3}$ and the insulator thickness is 5 nm. The gate length $L = 0.25\ \mu m$ while the gate width is $W = 2.5\ \mu m$. The inversion layer mobility for the MOSFET is $\mu_N = 250\ cm^2/V \cdot s$.



A capacitance voltage curve of the n^+ poly-silicon gate MOSFET was taken by connecting the source, drain and body terminals together. A voltage was applied between the gate and the body.



With the device biased as follows: $V_{BS} = 0\ V$, $V_{DS} = 0.1\ V$, $V_{GS} = 1.11\ V$, answer the following questions:

(1a) *(5 points)* Calculate the sheet charge density at the drain end of the device, $Q_n(y = L)$ *(numerical answer expected).*

At this bias point, the device is in the linear regime (small V_{DS}). In consequence, at the drain end, Q_n is given by:

$$Q_n(y=L) = -C_{ox}(V_{GD} - V_T)$$

we need to evaluate C_{ox}:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-13}\ F/cm}{5 \times 10^{-7}\ cm} = 6.9 \times 10^{-7}\ F/cm^2$$

V_T can be extracted from the C-V figure: 0.11 V. Then

$$Q_n(y=L) = -6.9 \times 10^{-7} \frac{F}{cm^2}(1.01 - 0.11) = -6.2 \times 10^{-7}\ C/cm^2$$

(1b) *(5 points)* Calculate the electron drift velocity at the drain end of the device, $v_n(y = L)$ *(numerical answer expected).*

The electron velocity is fairly uniform along the channel since V_{DS} is very small. Then:

$$v_n(y=L) = \mu_n \mathcal{E}_n(y=L) \simeq \mu_n \frac{V_{DS}}{L} = 250\ cm^2/V\text{-}s\ \frac{0.1\ V}{0.25 \times 10^{-4}\ cm} =$$

$$= 10^6\ cm/s$$

(1c) *(5 points)* Calculate the electron drift velocity in the middle of the channel $v_n(y = L/2)$ *(numerical answer expected).*

Same as above. Electron velocity is very uniform along the channel for small V_{DS}:

$$v_n\left(y=\frac{L}{2}\right) \simeq v_n(y=L) = 10^6\ cm/s$$

(1d) *(5 points)* This device is now desired to operate at $V_{DS} = 1.8\ V$ and $V_{GS} = 1.35\ V$ with a current $I_D = 1\ mA$. This requires shifting the threshold voltage V_T by means of an applied body voltage, V_{BS}. What is V_T in this situation? *(Numerical answer expected).*

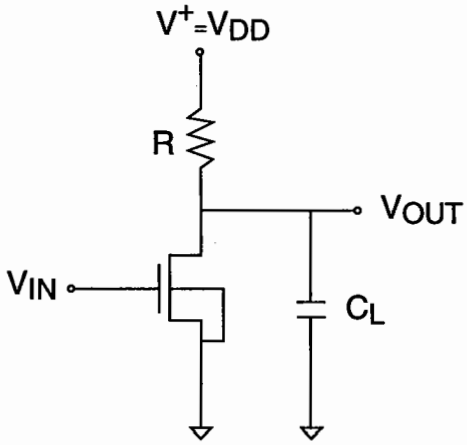
V_{DS} is high so the device is likely to be in the saturation regime. We need to find the value of V_T that is required to deliver this current. From the current equation in the saturation regime:

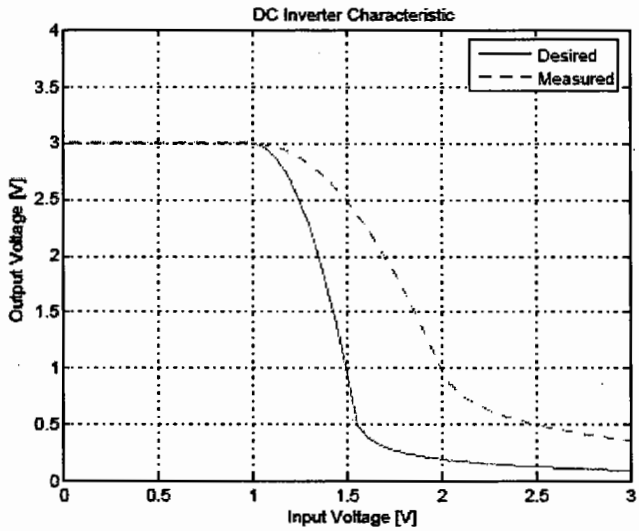
$$I_D = \frac{W}{2L} \mu_n C_{ox} \left[V_{GS} - V_T(V_{BS}) \right]^2$$

we can solve for V_T:

$$V_T(V_{BS}) = V_{GS} - \sqrt{\frac{2L I_D}{W \mu_n C_{ox}}} = 1.35 - \sqrt{\frac{2 \times 0.25 \times 10^{-4} \times 10^{-3}}{2.5 \times 10^{-4} \times 250 \times 6.9 \times 10^{-3}}} = 0.27\ V$$

2. *(30 points)* The circuit diagram for an NMOS inverter driving a load capacitance C_L, and a graph of its static input-output characteristics, are shown below. The graph actually shows two sets of characteristics, the desired characteristics and the measured characteristics. The two are different because the actual inverter was not fabricated exactly as it was designed. The point of this problem is to determine what went wrong during fabrication.





The circuit parameters under suspicion are the MOSFET gate width to length ratio, W/L, the MOSFET gate oxide thickness, t_{ox}, the MOSFET body doping level, N_a, and the pull-up resistance, R. Further, assume that one and only one of these four parameters was incorrectly fabricated.

(2a) *(3 points)* From the graph of the desired characteristics, estimate the *desired* threshold voltage V_T of the MOSFET *(numerical answer expected).*

V_T is the input voltage at which the transfer characteristics start going down. That seems to be around 1 V for the desired characteristics.

(2b) *(3 points)* From the graph of the measured characteristics, estimate the *actual* threshold voltage V_T of the MOSFET *(numerical answer expected).*

Still, also 1 V for the measured characteristics.

(1e) *(5 points)* For the bias conditions of (1d), compute the sheet charge density at the source end of the channel $Q_n(y=0)$ *(numerical answer expected).*

This is simply given by:

$$Q_n(y=0) = -C_{ox}\left[V_{GS} - V_T(V_{BS})\right] =$$

$$= -6.9\times10^{-7}\,(1.35 - 0.27) = -7.5\times10^{-7}\ \text{C/cm}^2$$

(1f) *(5 points)* For the bias conditions of (1d), calculate the electron drift velocity at the source end of the channel, $v_n(y=0)$ *(numerical answer expected).*

Since

$$I_D = -W Q_n(y=0)\, v_n(y=0)$$

Then

$$v_n(y=0) = \frac{I_D}{-W Q_n(y=0)} = \frac{10^{-3}\ \text{A}}{+2.5\times10^{-4}\ \text{cm} \times 7.5\times10^{-7}\ \frac{\text{C}}{\text{cm}^2}} = 5.3\times10^{6}\ \text{cm/s}$$

(2c) *(3 points)* From the graph of the desired characteristics, estimate the product of the desired pull-up resistance R and the desired K parameter of the MOSFET (where $K = \frac{W}{L}\mu_n C_{ox}$). That is, estimate the *desired* product RK *(numerical answer expected).*

When V_{IN} increases right above threshold, the MOSFET turns on in saturation. As V_{IN} exceeds V_T, V_{OUT} drops quickly. We can easily estimate RK by examining this regime.

With the MOSFET in saturation, we have:

$$V_{OUT} = V_{DD} - R I_D = V_{DD} - R \frac{W}{2L} \mu_n C_{ox} (V_{IN} - V_T)^2$$

where $V_{GS} = V_{IN}$. Then

$$R \frac{W}{L} \mu_n C_{ox} = \frac{2(V_{DD} - V_{OUT})}{(V_{IN} - V_T)^2}$$

Let us select a point right above threshold, say

$$V_{IN} = 1.5\,V \rightarrow V_{OUT} = 1\,V$$

Substituting:

$$RK = \frac{2(3-1)}{(1.5-1)^2} = 16 \quad V^{-1}$$

(2d) *(3 points)* From the graph of the measured characteristics, estimate the product of the actual pull-up resistance R and the actual K parameter of the MOSET (where $K = \frac{W}{L}\mu_n C_{ox}$). That is, estimate the *actual* product RK *(numerical answer expected).*

we repeat the procedure of (2c) now for the actual characteristics, we select:

$$V_{IN} = 1.5\ V \quad \rightarrow \quad V_{OUT} = 2.5\ V$$

Then:

$$RK = \frac{2(3-2.5)}{(1.5-1)^2} = 4 \quad V^{-1}$$

In answering the following questions, remember to assume that one and only one of the four parameters was incorrectly fabricated.

(2e) *(3 points)* Could the gate width to length ratio, W/L, have been incorrectly fabricated? Why or why not? If "Yes", is it too big or too small? *(Appropriate explanation expected).*

Circle One: (Yes) No

it is clear that K_R has changed and this is one of the factors inside K.

K_R has come down. Hence W/L, if this is the problem, must have gotten smaller.

(2f) *(3 points)* Could the gate oxide thickness, t_{ox}, have been incorrectly fabricated? Why or why not? If "Yes", is it too big or too small? *(Appropriate explanation expected).*

Circle One: Yes (No)

V_T has not changed. t_{ox} affects V_t.

(2g) *(3 points)* Could the body doping density, N_a, have been incorrectly fabricated? Why or why not? If "Yes" is it too big or too small? *(Appropriate explanation expected).*

Circle One: Yes (No)

V_T has not changed. N_a affects V_T.

(2h) *(3 points)* Could the pull-up resistance, R, have been incorrectly fabricated? Why or why not? If "Yes" is it too big or too small? *(Appropriate explanation expected).*

Circle One: (Yes) No

R_K has gone down. This could be due to R going down.

You observe that when the inverter is driving a known load capacitance C_L, one of the propagation delays (t_{PLH} and t_{PHL}) is not as desired. In particular, the propagation delay from a rising input to a falling output is longer than expected, while the propagation delay from a falling input to a rising output is exactly what was expected.

(2i) *(6 points)* Based on all available evidence, which circuit parameter was incorrectly fabricated? What is the ratio of the actual parameter divided by the desired parameter? *(Appropriate explanation expected).*

The rising input to falling output transient is dominated by discharge of the capacitor through the transistor. Hence W/L is the suspect parameter. With this transient having slowed down, that suggests that W/L has gotten smaller, i.e., the transistor has less current drive. That is consistent with the answer to part (2e).

As for the ratio of the actual vs. desired, that has to be 1/4 since R/C has gone down by a factor of 4.

3. *(24 points)* An pn diode at a certain forward bias point is characterized by the following values of small-signal equivalent circuit elements:

$$r_d = 25\ \Omega \qquad C_d = 40\ pF$$

At this bias point, the depletion capacitance is negligible with respect to the diffusion capacitance.

In the following questions, you are asked to estimate how the values of these two elements change if the diode is modified in several ways. Assume that in all cases, the diode is ideal, very asymmetric, and that all its behavior is dominated by its lowly doped side. State any other assumptions you need to make.

(3a) *(4 points)* The diode area is doubled. Nothing else is changed. The diode is biased at the *same current* as in the problem statement *(numerical answers expected).*

r_d is given by:

$$r_d = \frac{nT}{qI}$$

At constant current, r_d does not change. Hence:

$$r_d' = r_d = 25\ \Omega$$

C_d is given by:

$$C_d = \frac{\tau_T}{r_d}$$

τ_T is independent of bias. Hence, at constant current r_d does not change and C_d does not change. Thus

$$C_d' = C_d = 40\ pF$$

(3b) *(4 points)* The diode area is doubled. Nothing else is changed. The diode is biased at the *same voltage* as in the problem statement *(numerical answers expected).*

If the diode area doubles, at the same voltage, the diode has twice as much current. Then:

$$I' = 2I$$

Therefore:

$$r_d' = \frac{nT}{qI'} = \frac{nT}{q2I} = \frac{nT}{qI}\frac{1}{2} = 12.5\ \Omega$$

τ_T does not depend on area. Then:

$$C_d' = \frac{\tau_T}{r_d'} = \frac{\tau_T}{r_d}2 = 80\ \mu F$$

(3c) *(4 points)* The doping level of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same current* as in the problem statement *(numerical answers expected).*

At the same current level r_d does not change. Then

$$r_d' = r_d = 25\ \Omega$$

To the first order, τ_T does not depend on the doping level. Hence, as in (3a):

$$C_d' = C_d = 40\ pF$$

To the second order, high doping level reduces the minority carrier diffusion coefficient which increases τ_T and C_d. For a factor of 2 changed in doping level, this is not very significant.

(3d) *(4 points)* The doping level of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same voltage* as in the problem statement *(numerical answers expected).*

if the doping level on the lowly doped side doubles, then I_0 of the diode goes down by a factor of 2. Then at the same voltage, I through the diode also drops by a factor of 2. Then

$$I' = \frac{I}{2}$$

and

$$r_d' = 2r_d = 50\,\Omega$$

τ_T is to first order independent of doping level. Then, to first order

$$C_d' = \frac{\tau_T}{r_d'} = \frac{\tau_T}{2r_d} = \frac{C_d}{2} = 20\ \text{pF}$$

(3e) *(4 points)* The thickness of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same current* as in the problem statement *(numerical answers expected).*

At the same current level, r_d does not change:

$$r_d' = r_d = 25\ \Omega$$

τ_T does depend on the thickness of the lowly doped side. The dependence is quadratic. Then

$$\tau_T' = \tau_T \left(\frac{W'}{W}\right)^2 = 4\,\tau_T$$

Then, at constant current:

$$C_d' = \frac{\tau_T'}{r_d'} = \frac{4\tau_T}{r_d} = 4\,C_d = 160\ \mu F$$

(3f) *(4 points)* The thickness of the lowly doped side is doubled. Nothing else is changed. The diode is biased at the *same voltage* as in the problem statement *(numerical answers expected).*

If the thickness of the lowly doped side is doubled, then I_0 of the diode goes down by a factor of 2. Hence, at constant voltage, I also goes down by a factor of 2. Then

$$r_d' = 2 r_d = 50\ \Omega$$

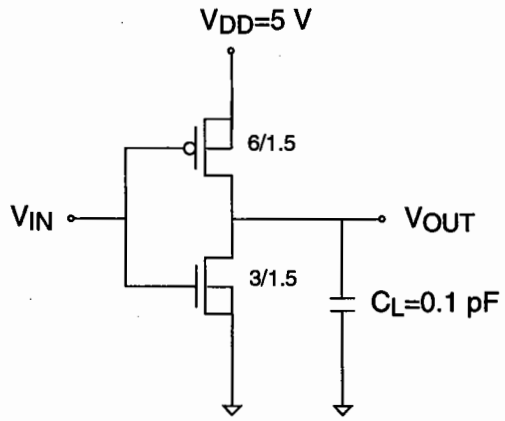
As in part (3e):

$$\tau_i' = 4 \tau_i$$

Then, at constant voltage:

$$C_d' = \frac{\tau_i'}{r_d'} = \frac{4 \tau_i}{2 r_d} = 2 C_d = 80\ \mu F$$

4. *(16 points)* Consider a CMOS logic gate driving a capacitive load C_L. The inverter is made with minimum size transistors, as sketched below:



In the above diagram, the two numbers next to each transistor give its gate dimensions (width/length) in microns. In solving this problem, assume that C_L is the dominant capacitance in this circuit. All other capacitances can be neglected next to C_L.

The technology is defined by the following circuit parameters plus other geometrical parameters:

Parameter Name	HSPICE Symbol	NMOS	PMOS	units
Zero bias threshold voltage	VTO	0.75	-0.75	V
Oxide thickness	TOX	1.5E-08	1.5E-08	m
Transconductance parameter μC_{ox}	KP	100E-06	50E-06	A/V^2
Channel-length modulation parameter	LAMBDA	7E-02$\frac{1.5}{L(\mu m)}$	7E-02$\frac{1.5}{L(\mu m)}$	V^{-1}
Zero bias planar bulk depletion capacitance	CJ	1E-04	3E-04	F/m^2
Zero bias sidewall bulk depletion capacitance	CJSW	5E-10	3.5E-10	F/m
Bulk junction potential	PB	0.9	0.9	V
Planar bulk junction grading coefficient	MJ	0.5	0.5	dimensionless
Sidewall bulk junction grading coefficient	MJSW	0.33	0.33	dimensionless
Diffusion length	L_{diff}	4.5	4.5	μm
Minimum transistor length	L_{min}	1.5	1.5	μm
Minimum transistor width	W_{min}	3	6	μm

(4a) *(8 points)* Estimate the energy stored in the load capacitor when the output is HI *(numerical answer expected).*

when the output is HI, the capacitor is charged to V_{DD}. Then, the energy stored in this capacitor is:

$$E_C = \frac{1}{2} C_L V_{DD}^2 = \frac{1}{2} 0.1 \times 10^{-12} F \cdot 25 V^2 = 1.3 \times 10^{-12} J$$

(4b) *(8 points)* Estimate the power dissipated by this inverter when it is run at 100 MHz *(numerical answer expected).*

Each full cycle, this circuit dissipates

$$E = 2E_C = 2.5 \times 10^{-12}\ \text{J}$$

At 100 MHz, the power consumption is

$$W = fE = 100 \times 10^6 \times 2.5 \times 10^{-12} = 0.25\ \text{mW}$$