Homework #7 - October 28, 2005

Due: November 4, 2005 at recitation (2 PM latest)
(late homework will not be accepted)

Please write your recitation session time on your problem set solution.

1. *[20 points]* Problem E4.19 of Howe & Sodini. Note comment before exercise E4.1 in page 246 of Howe & Sodini.

2. *[40 points]* Problem P5.5 of Howe & Sodini. Note comment before exercise E5.1 in p. 319 of Howe & Sodini. Note also that in some versions of the book, there is an error in the list of parameters. λ_n and λ_p should be given by:

$$\lambda_n = \lambda_p = 0.067 \frac{1.5}{L} V^{-1}$$

with L in μm

3. *[40 points]* **Design the DC transfer function of an Asymmetric Inverter**

One goal of design project for 6.012 is to expose students to the design of integrated circuits using a modern design tool. It highlights the difference between design and analysis. The project requires the use of the Cadence suite of design tools. This homework question gives you an opportunity to configure your Cadence setup and consider some of the design issues of the project in advance.

Modern digital chips run at 5 V, 3.3 V, 1.8 V, 0.9 V and voltages in between. Digital CMOS logic signals need to be converted from one voltage level to another when you switch operating voltages. In this question you will design a CMOS inverter to convert from 3.3 V to 5 V operation. To design an inverter means to select the W_p, L_p, W_n and L_n of the MOS devices.

The input signal of your inverter will go from 0 to 3.3 V, and the output from 0 to 5 V. For the best noise margin for the 3.3 V logic on the input side and the 5 V logic on

the output side we want the inverter designed so that $v_{OUT} = 5\ V \times 0.5 = 2.5\ V$ when $v_{IN} = 3.3\ V \times 0.5 = 1.65\ V$.

We are not considering the loading, rise/fall times or delay of this inverter. Design the inverter so that it is the minimum possible size. You might want to think about what you would have to do to scale it for a different load capacitor. You will be asked about this in next week's homework.

Use $V_{DD} = 5\ V$. Use the device models from the Cadence Tutorial. The minimum and maximum lengths are 1.5 μm and 100 μm with a 0.5 μm stepsize. The minimum and maximum widths are 3 μm and 100 μm with a 0.5 μm stepsize.

a) [30 points] From the Cadence tutorial you know how to use the dc simulation to sweep the input voltage and plot the dc transfer curve. Describe a procedure using Cadence to find the values of W_p, L_p, W_n and L_n that produce the desired inverter.

   Hint: You can sweep any design variable that you use in the schematic, not just power supplies.

b) [5 points] Use your method and find the W_n, L_n, W_p and L_p that produce the desired inverter. Give the design values for the following parameters:

   W_p
   L_p
   W_n
   L_n
   $S_p = W_p/L_p$
   $S_n = W_n/L_n$
   $S_{inv} = S_p/S_n$

c) [5 points] Provide a plot of the DC transfer characteristic for your inverter. Show that the V_M point is at $v_{IN} = 1.65\ V$ and $v_{OUT} = 2.5\ V$.